

Monolithic Transformer-Coupled RF Power Amplifiers in Si-Bipolar

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Hans-Dieter Wohlmuth, Mirjana Rest, Klaus Aufinger, Arpad L. Scholtz¹

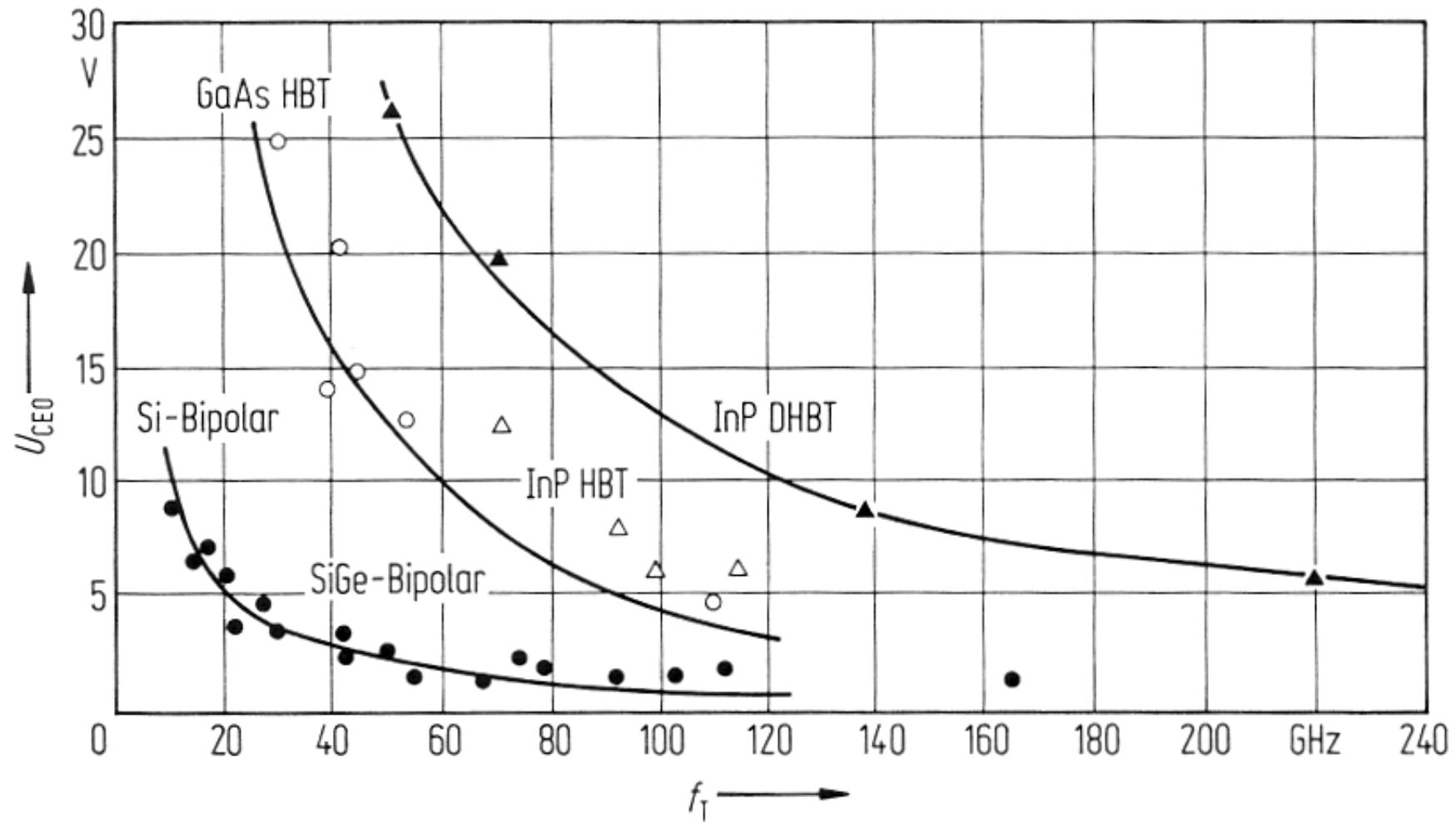
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and Radio Frequency Engineering, Austria

Outline

- ▶ Introduction
- ▶ High Performance On-Chip Transformer Design
- ▶ A 2.5 V, 1 W Si-bipolar PA with 55 % PAE at 1.9 GHz
- ▶ A 2.8 V, 3.2 W Si-bipolar PA with 54 % PAE at 900 MHz
- ▶ Conclusion

BV_{CE0} versus Transit Frequency



Motivation & Challenges

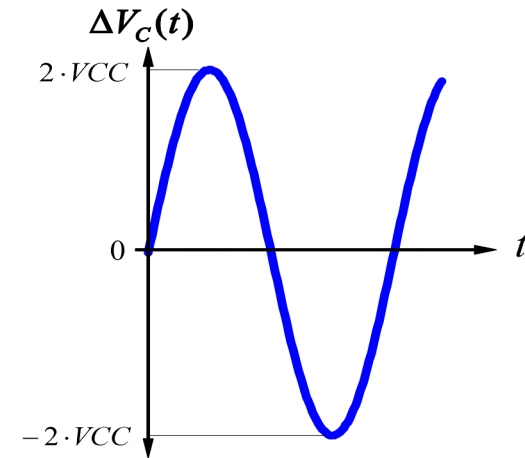
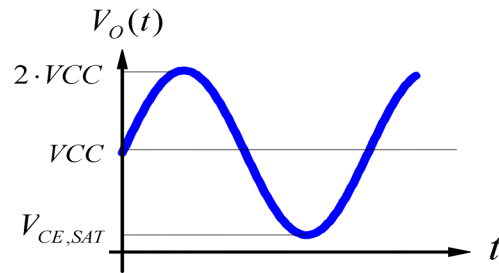
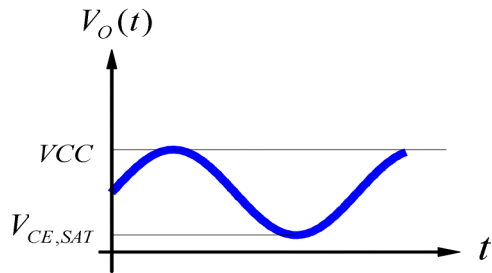
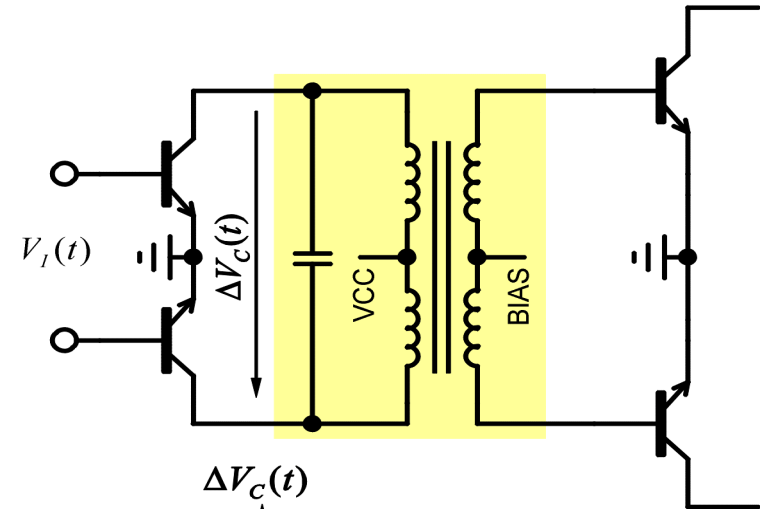
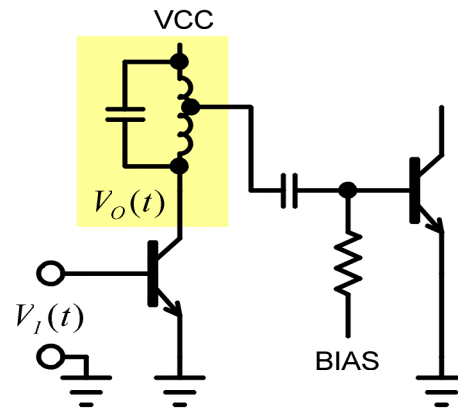
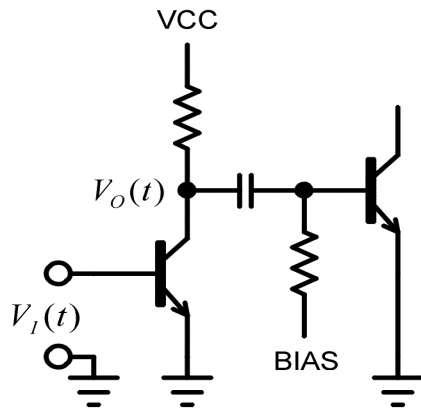
- ▶ high output power at very low supply voltages, e.g.:
0.5 W, 1.8 V, 2 GHz and **3 W, 2.8 V, 900 MHz**
- ▶ high efficiency > 50 %
- ▶ monolithic integration
- ▶ standard low-cost Si-bipolar technology

On-Chip Interstage Matching

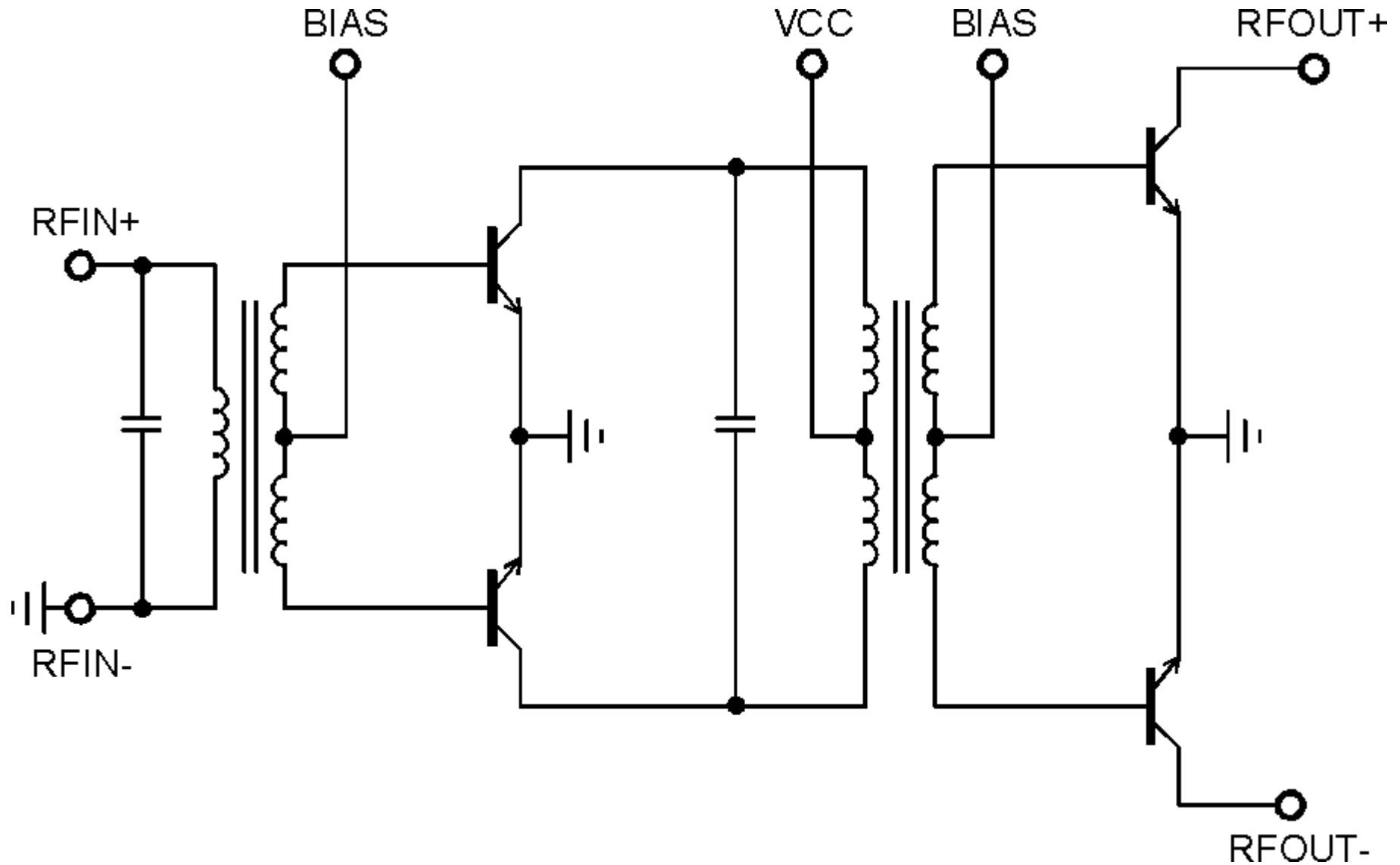
Conventional Design

On-Chip Inductance

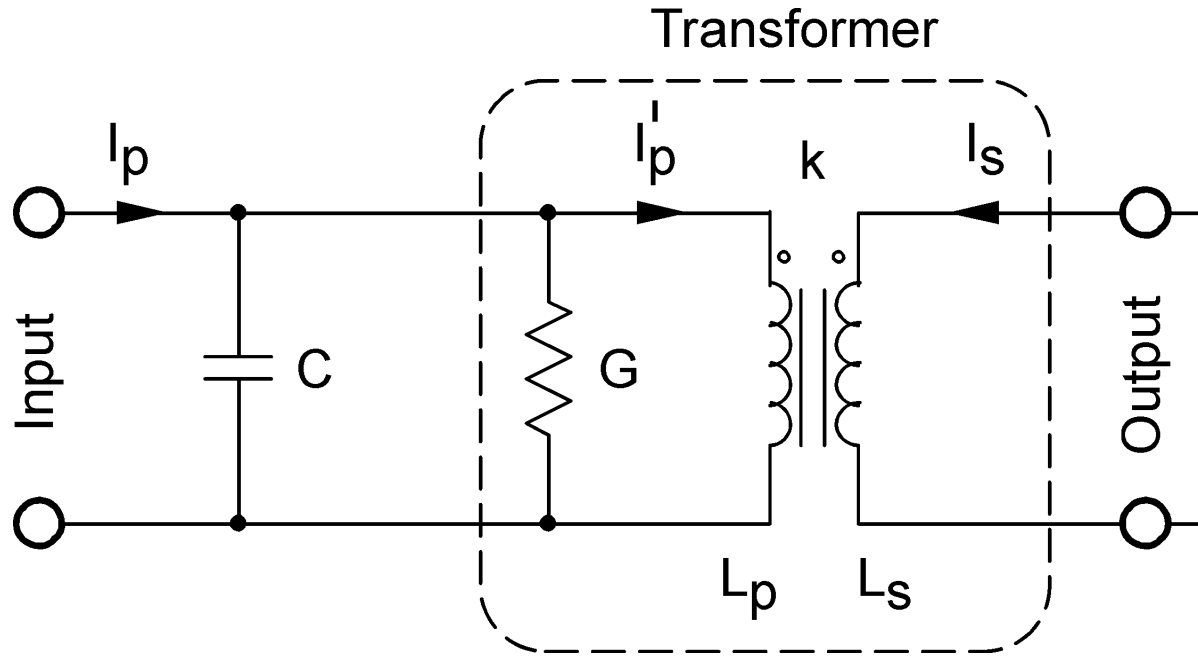
On-Chip Transformer



Push-Pull Type Power Amplifier



Current Transfer Ratio of a Lossy Tuned Transformer



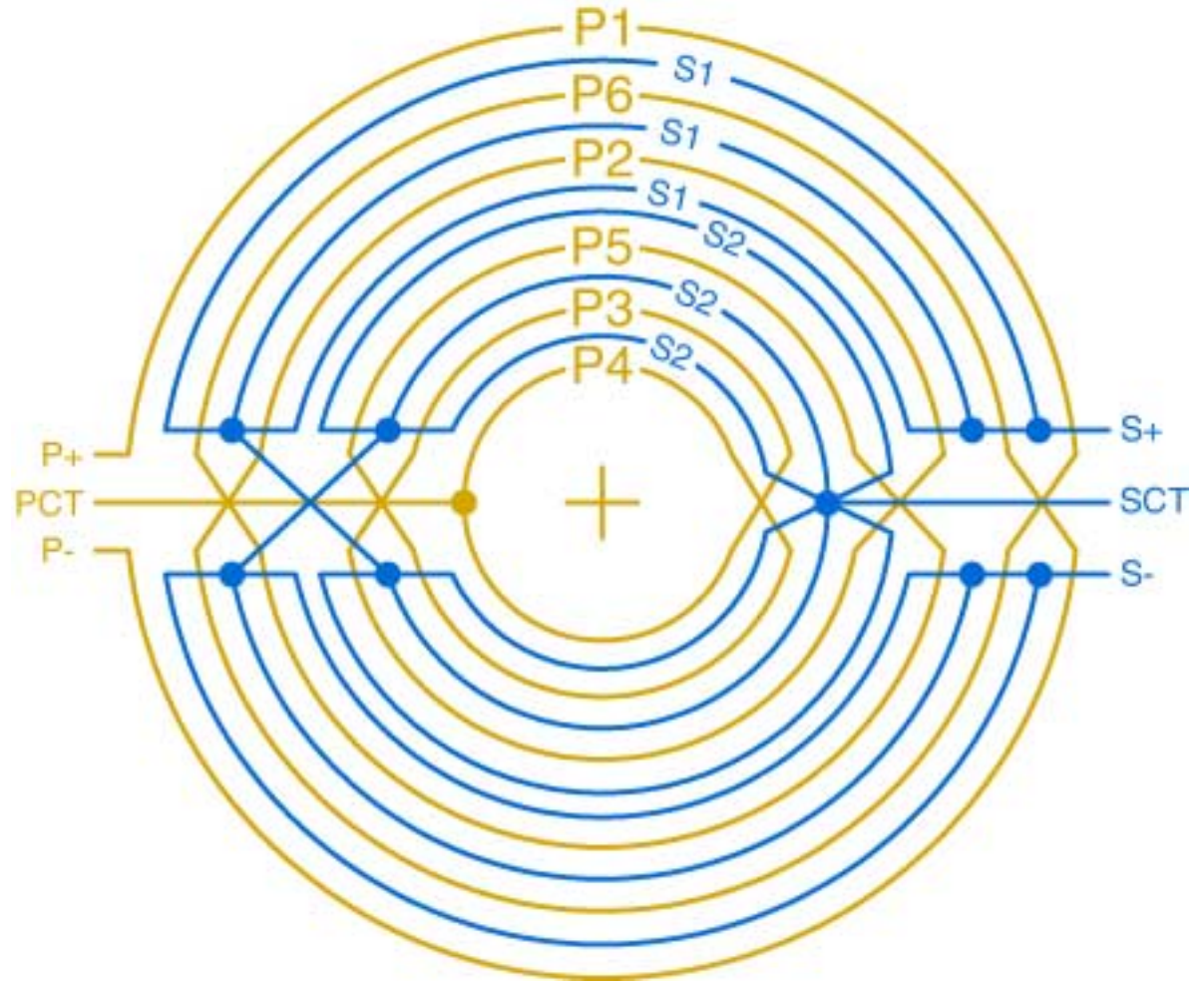
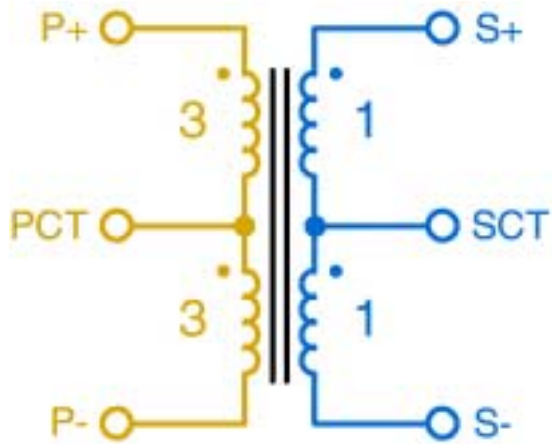
$$Q = \frac{\omega_{res} \cdot C}{G} = \frac{1}{G} \cdot \sqrt{\frac{C}{(1-k^2) \cdot L_p}}$$

$$\left| \frac{I_s}{I_p} \right| = k \cdot Q \cdot \sqrt{\frac{L_p}{L_s}}$$

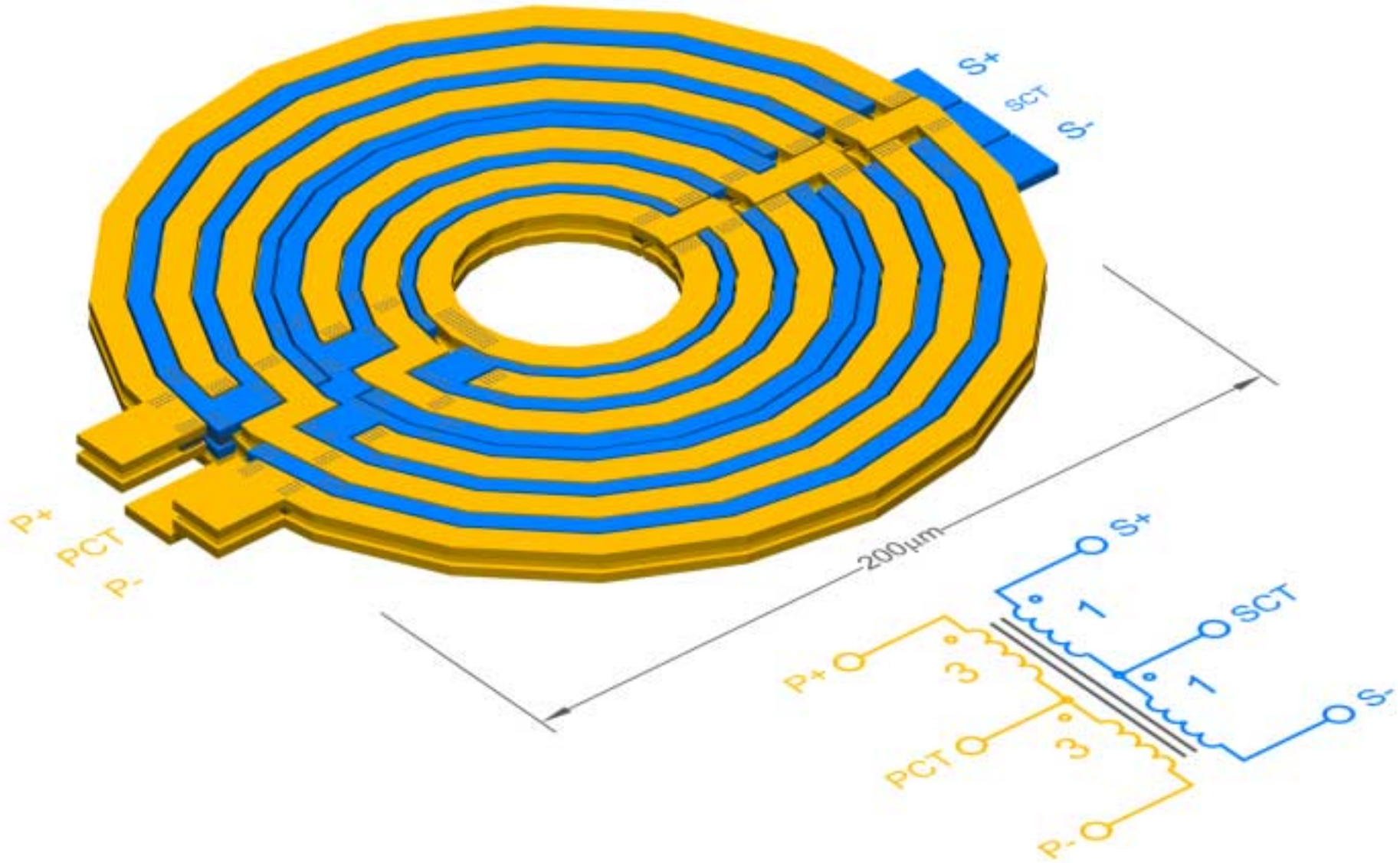
Monolithic Transformer Winding Scheme

Electrical Symbol

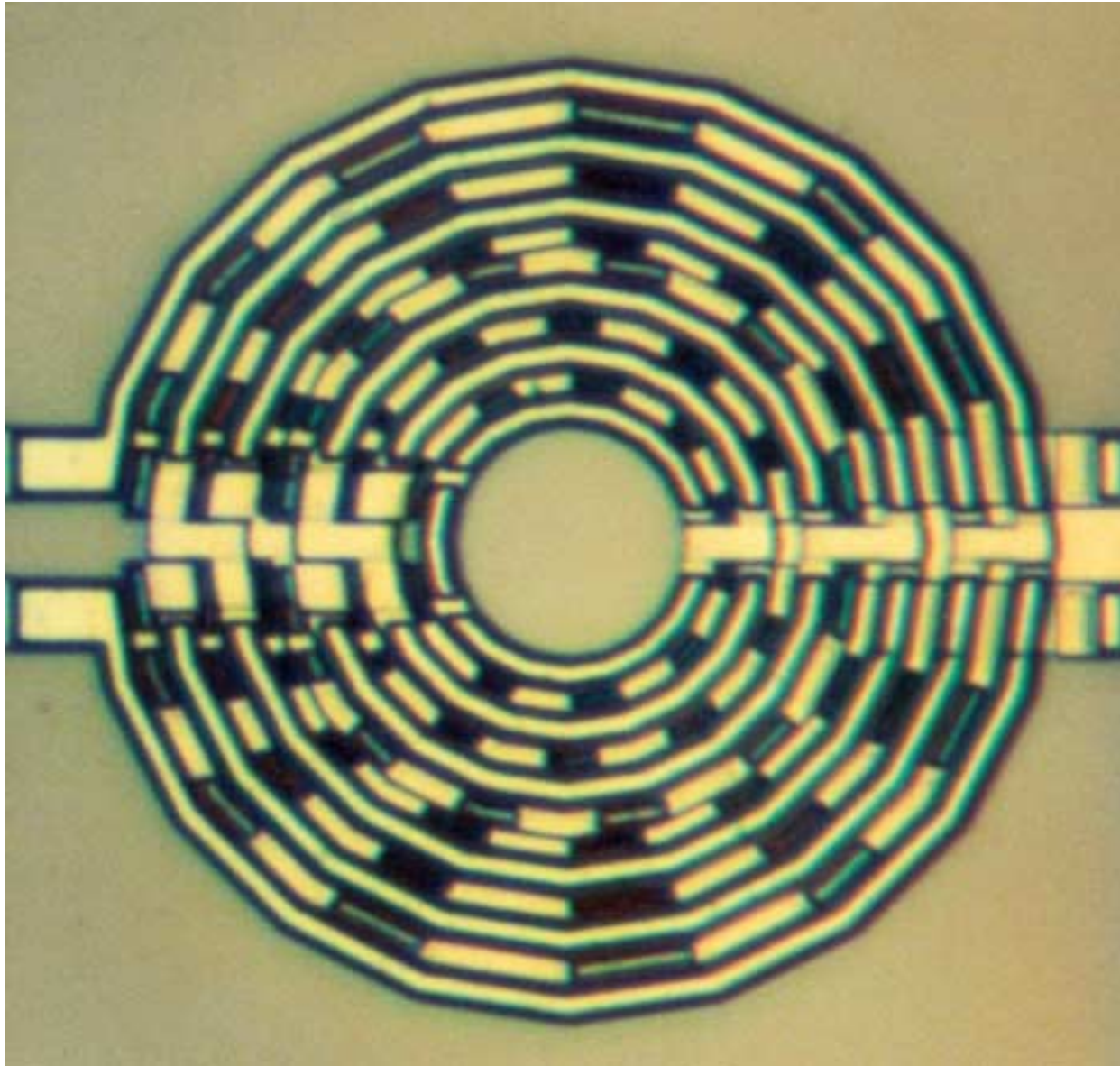
$$N = 6 : 2$$



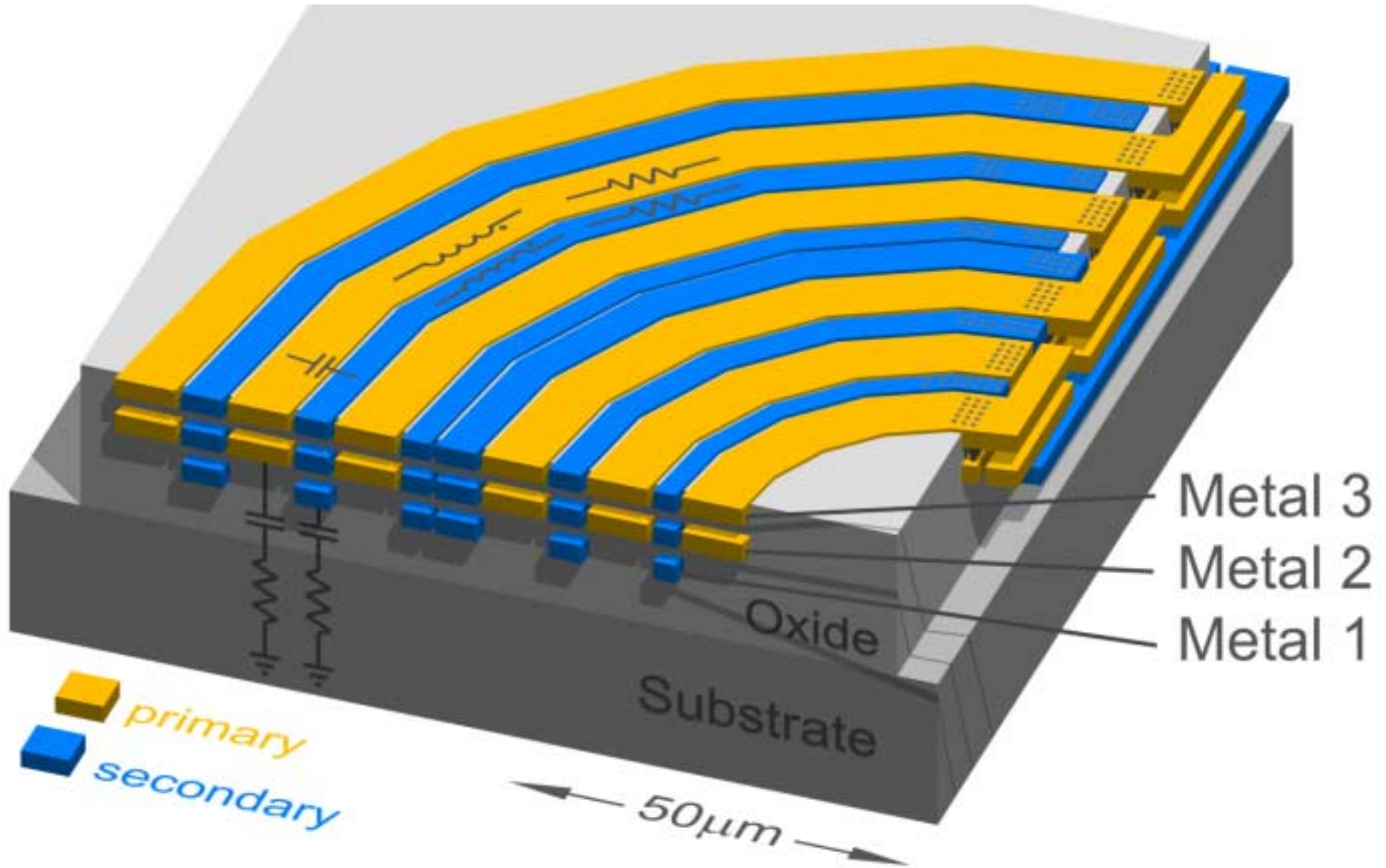
2 GHz Monolithic Transformer 3-D View



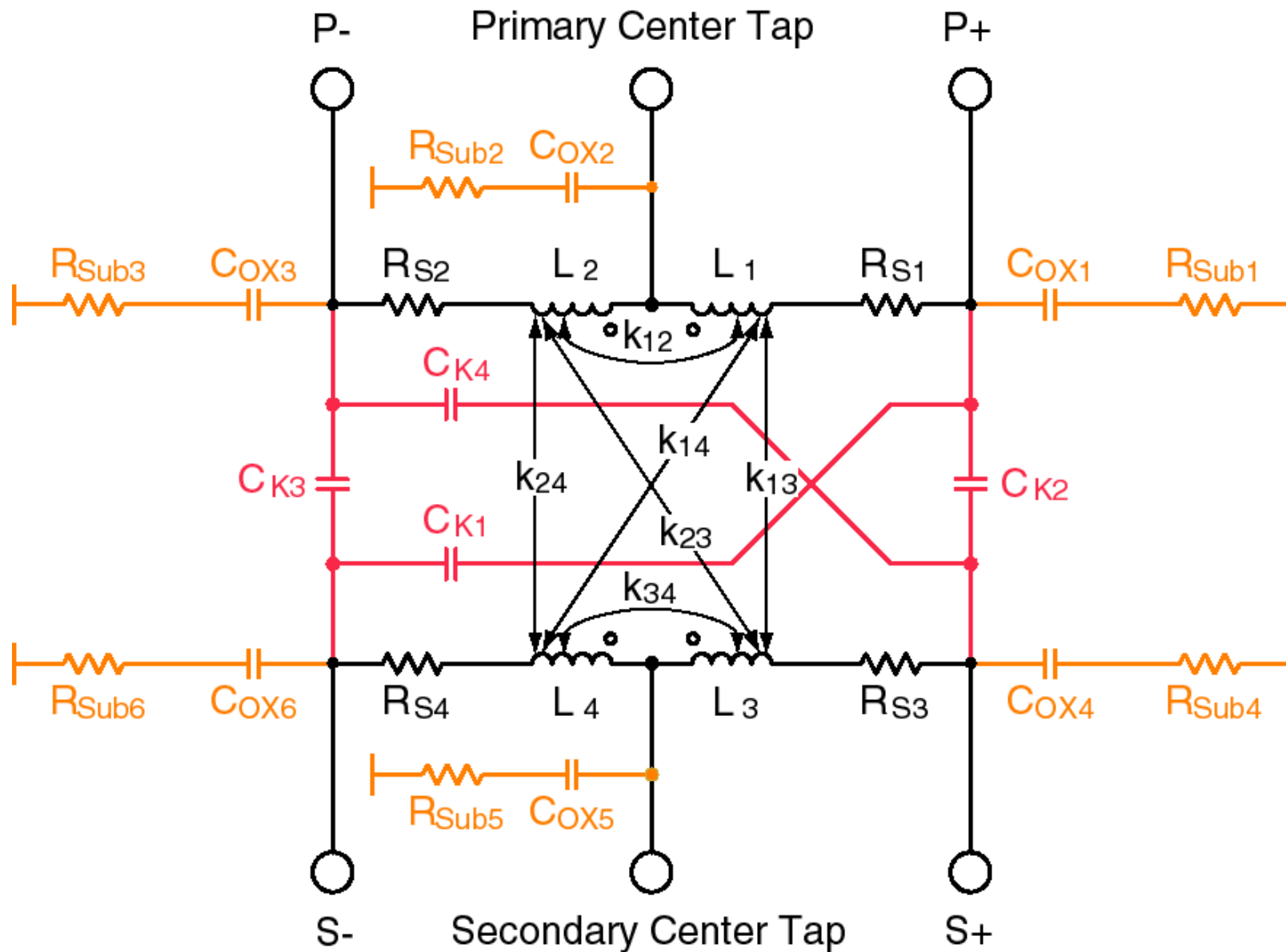
2 GHz Monolithic Transformer (\varnothing 200 μm)



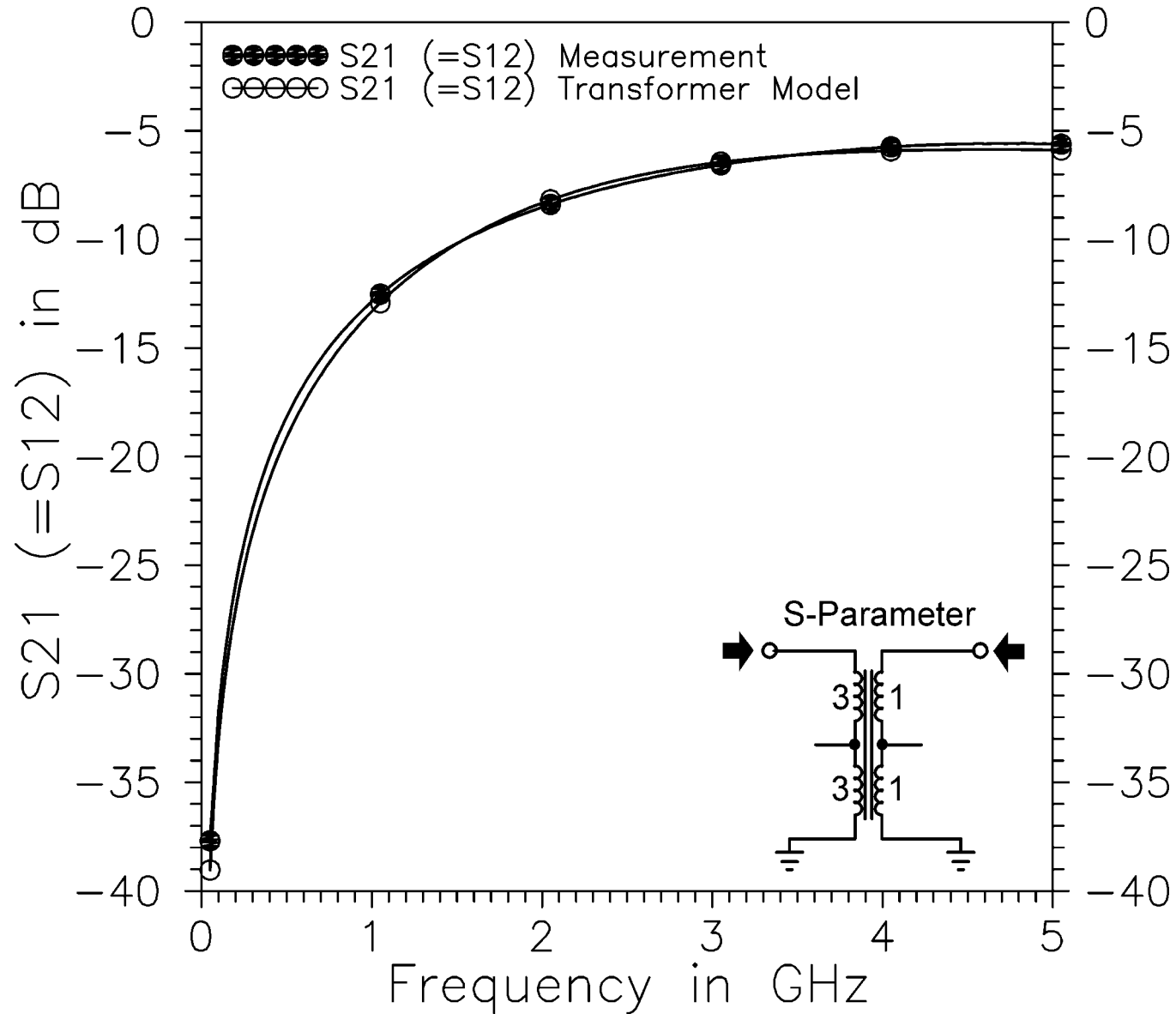
Transformer Cross Section



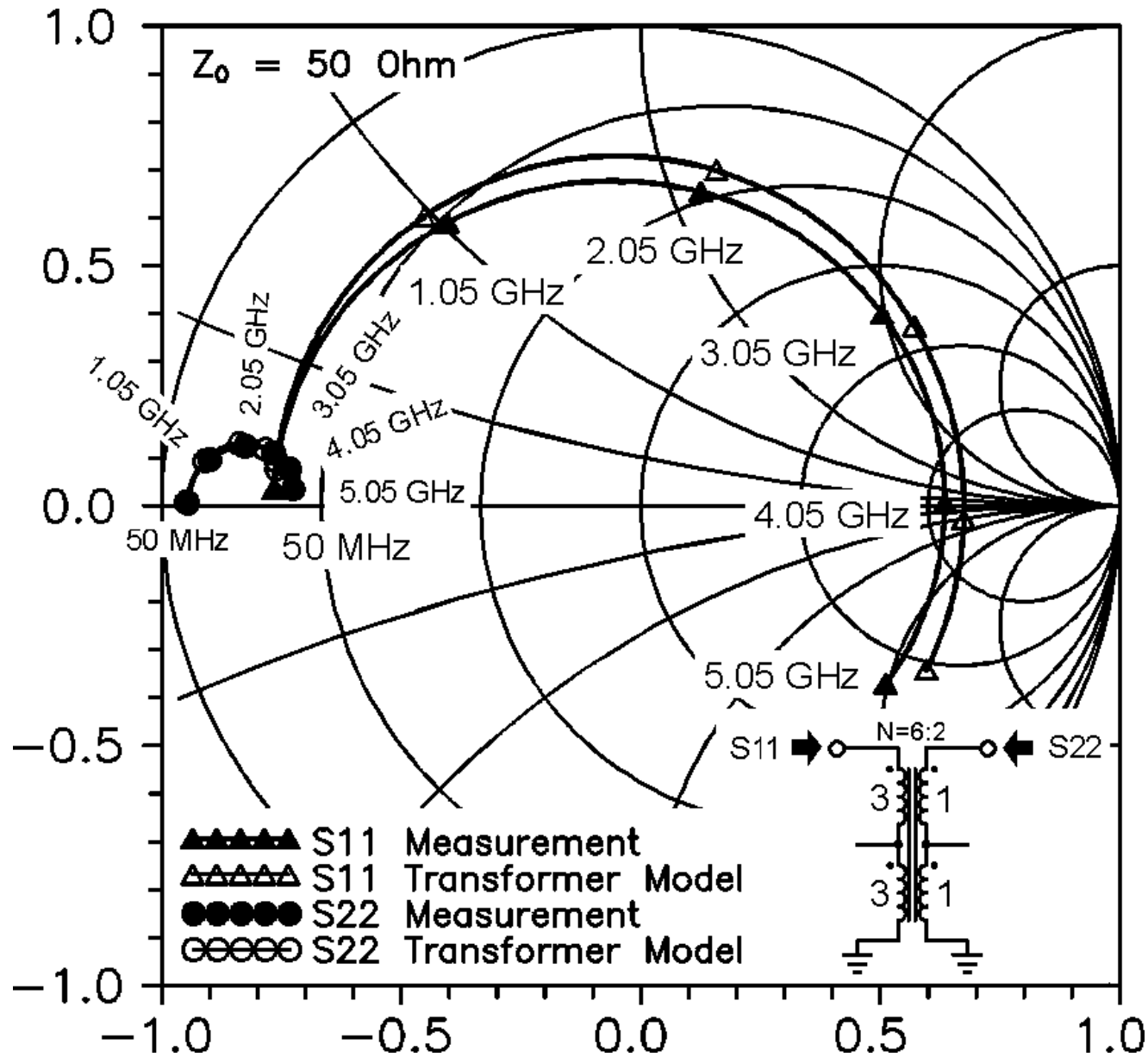
Lumped Planar Transformer Model



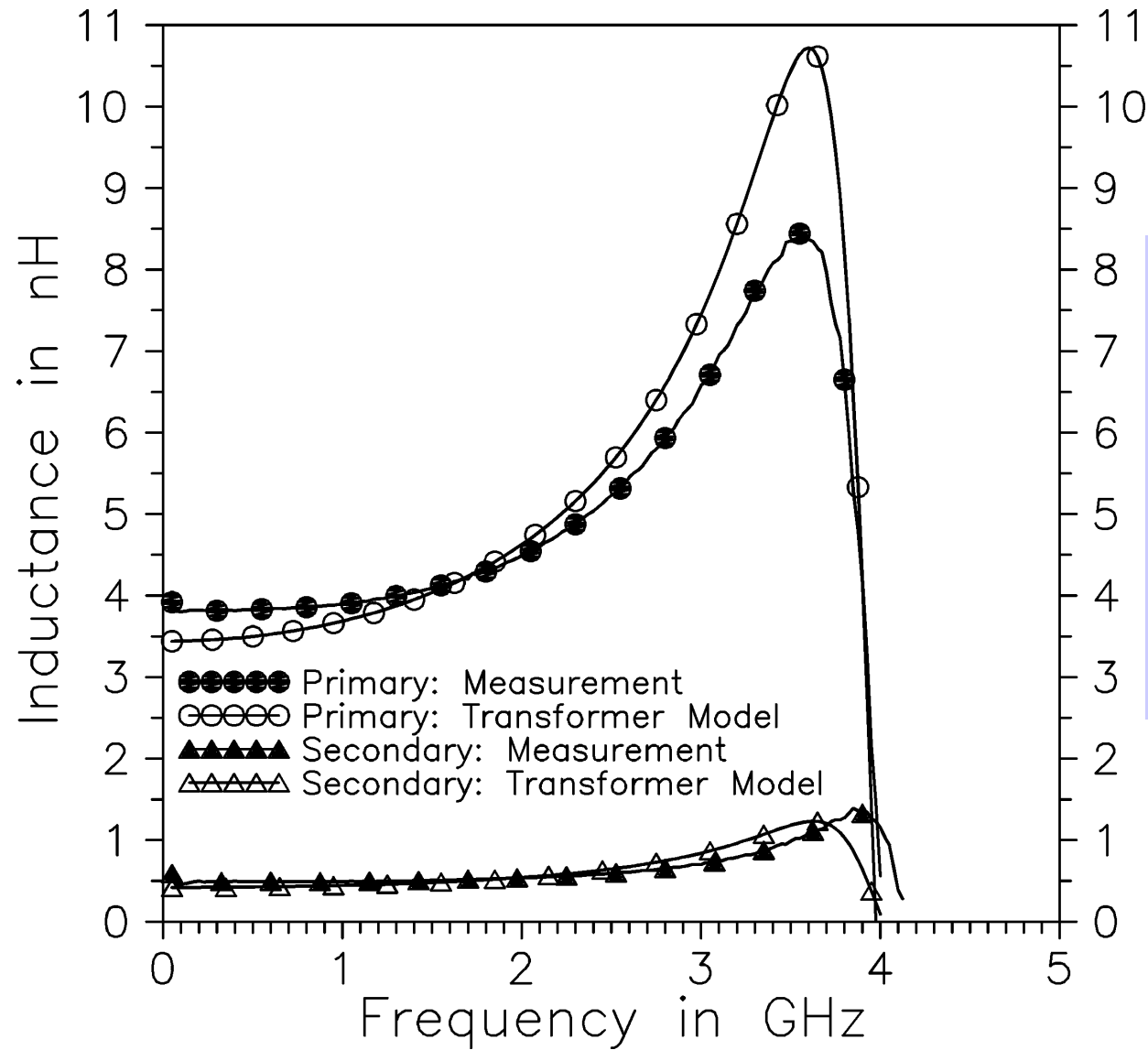
Transformer Transmission Coefficient



Transformer Reflection Coefficients



Transformer Inductance

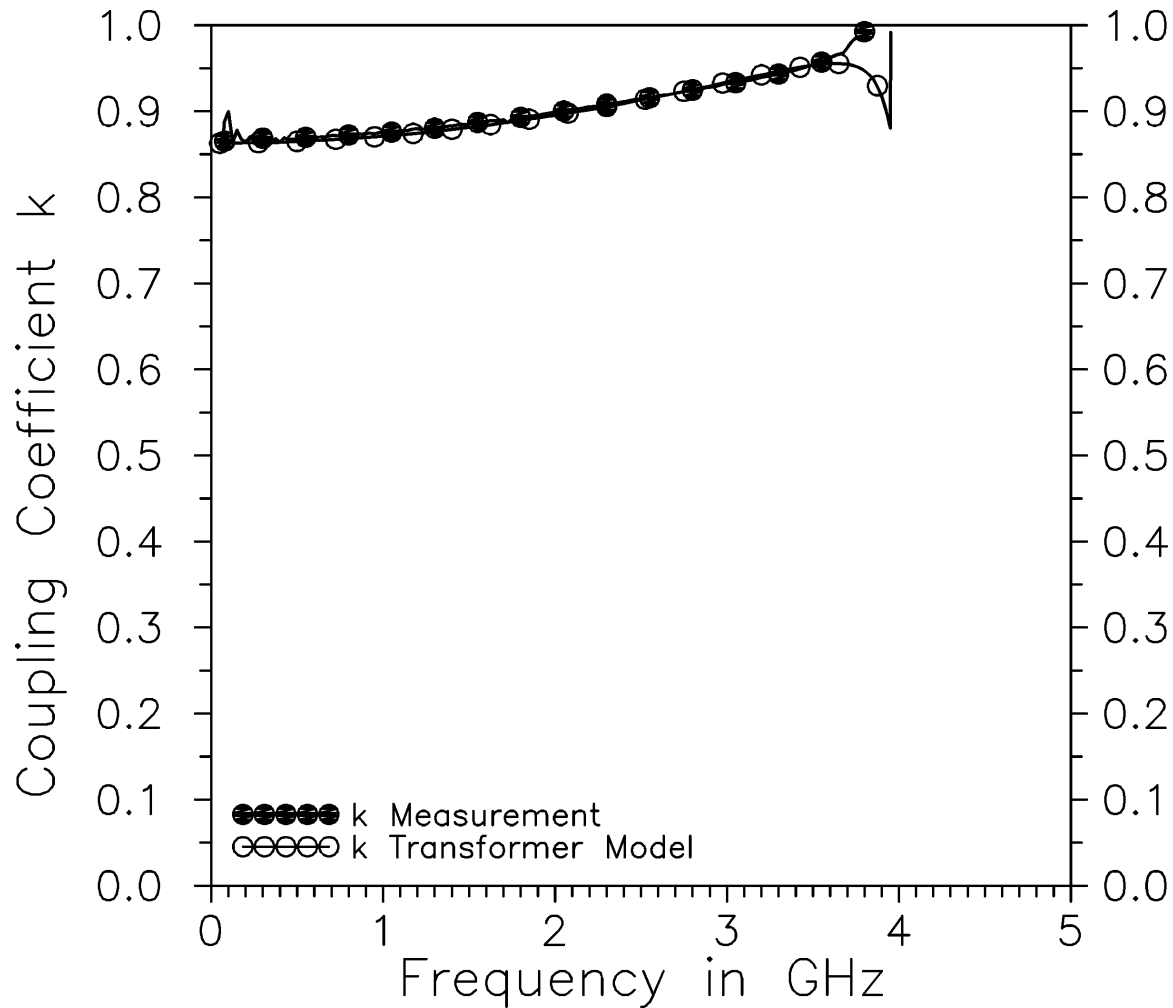


Inductance

$$L_P(\omega) = \frac{\text{Im}(Z_{11})}{\omega}$$

$$L_S(\omega) = \frac{\text{Im}(Z_{22})}{\omega}$$

Transformer Coupling Coefficient



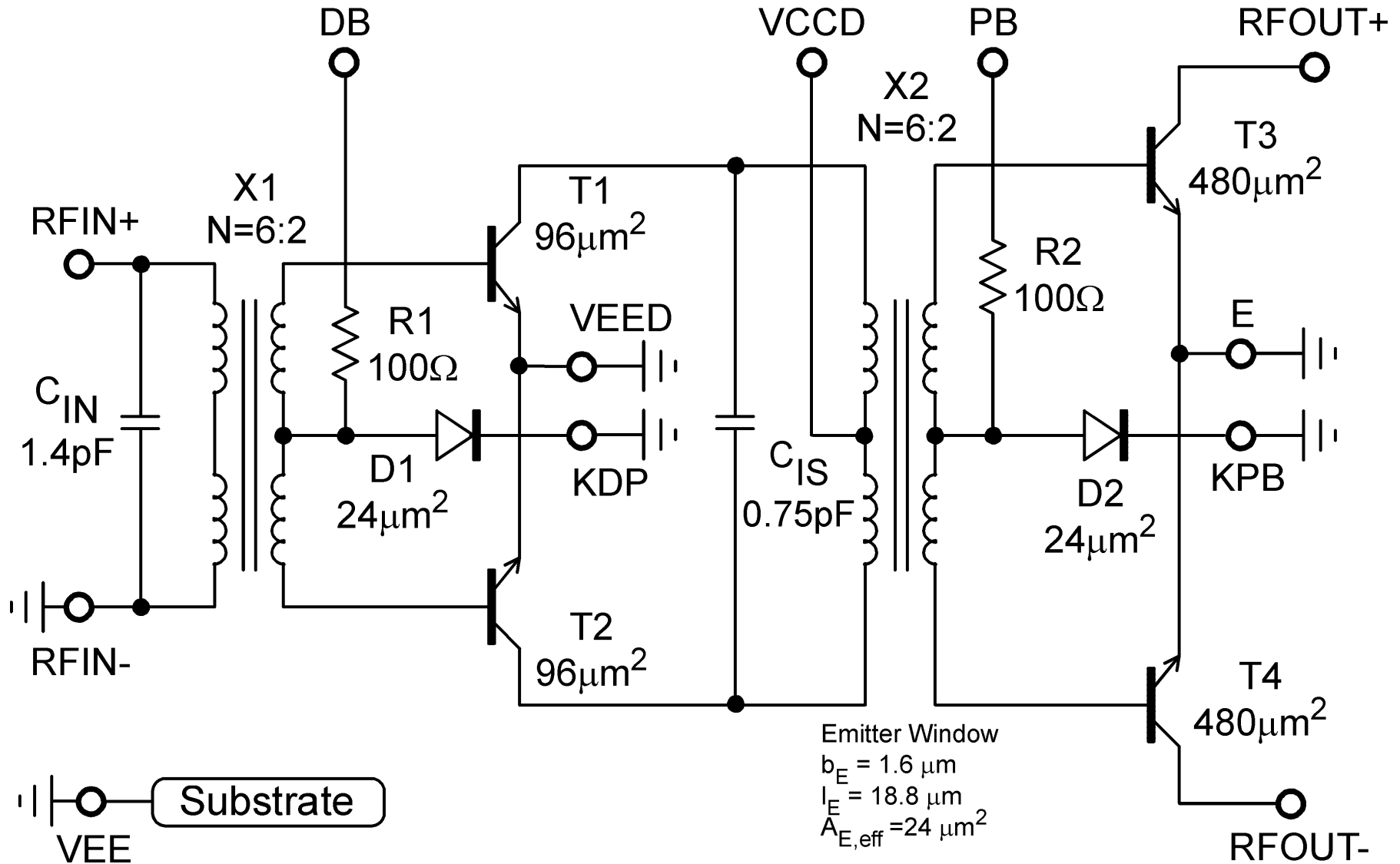
Coupling Coefficient

$$\begin{aligned}k_{LP,LS}(\omega) &= \sqrt{\frac{(Y_{11}^{-1} - Z_{11}) \cdot Z_{22}}{\text{Im}(Z_{11}) \cdot \text{Im}(Z_{22})}} \\ &= \sqrt{\frac{M^2 \cdot \omega^2}{\text{Im}(Z_{11}) \cdot \text{Im}(Z_{22})}} \\ &= \frac{M}{\sqrt{L_P \cdot L_S}}\end{aligned}$$

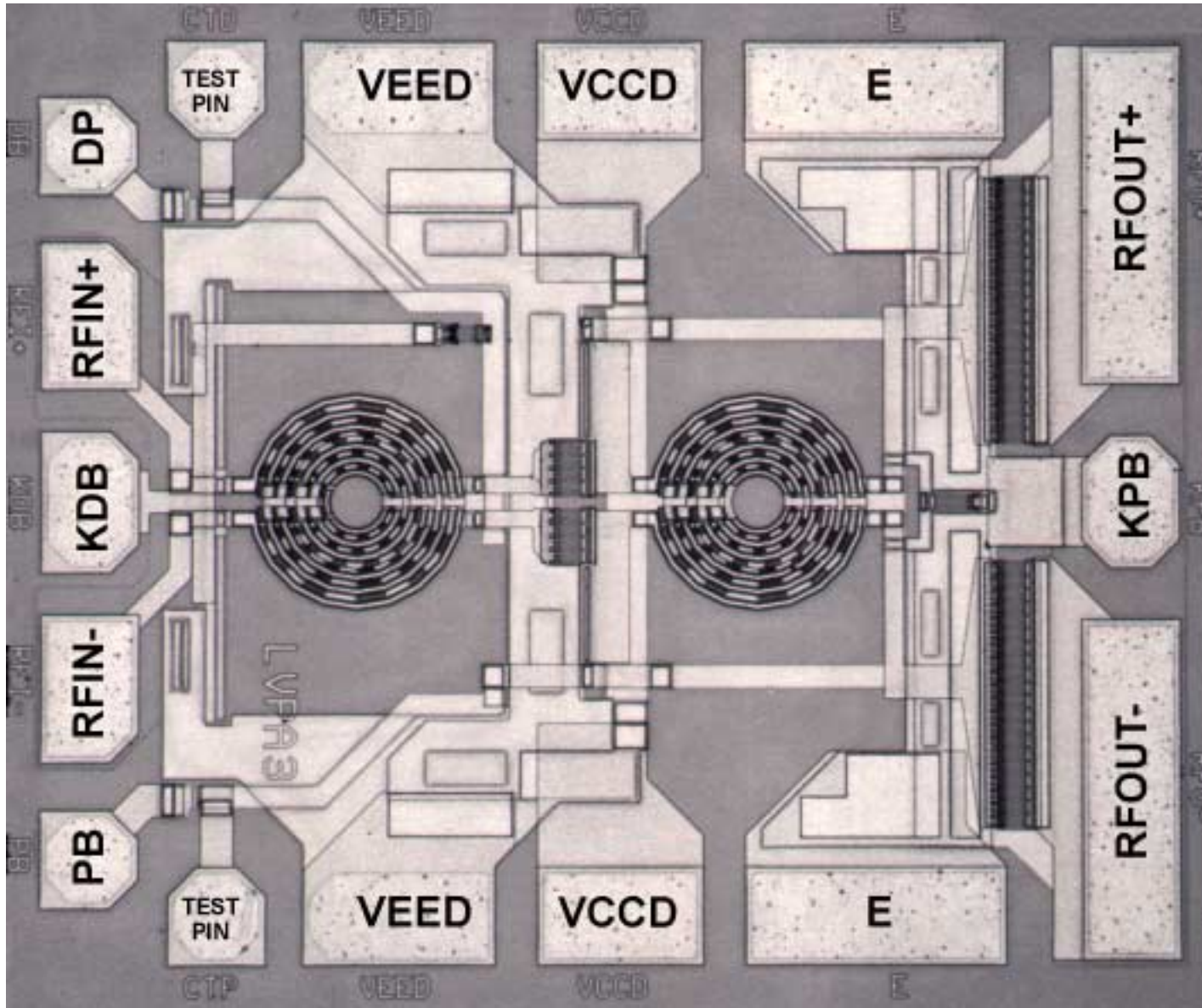
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- ▶ Conclusion

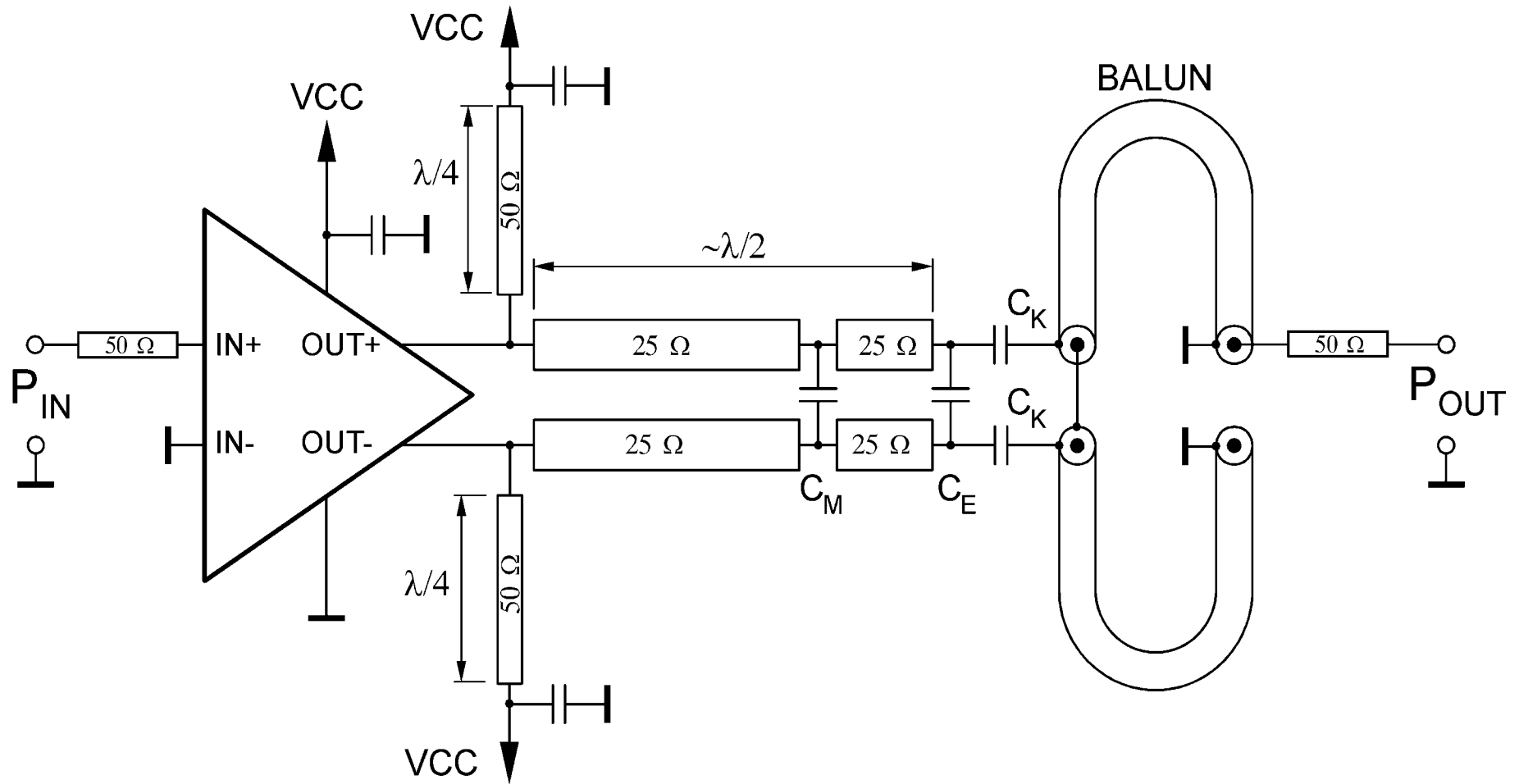
Circuit Diagram



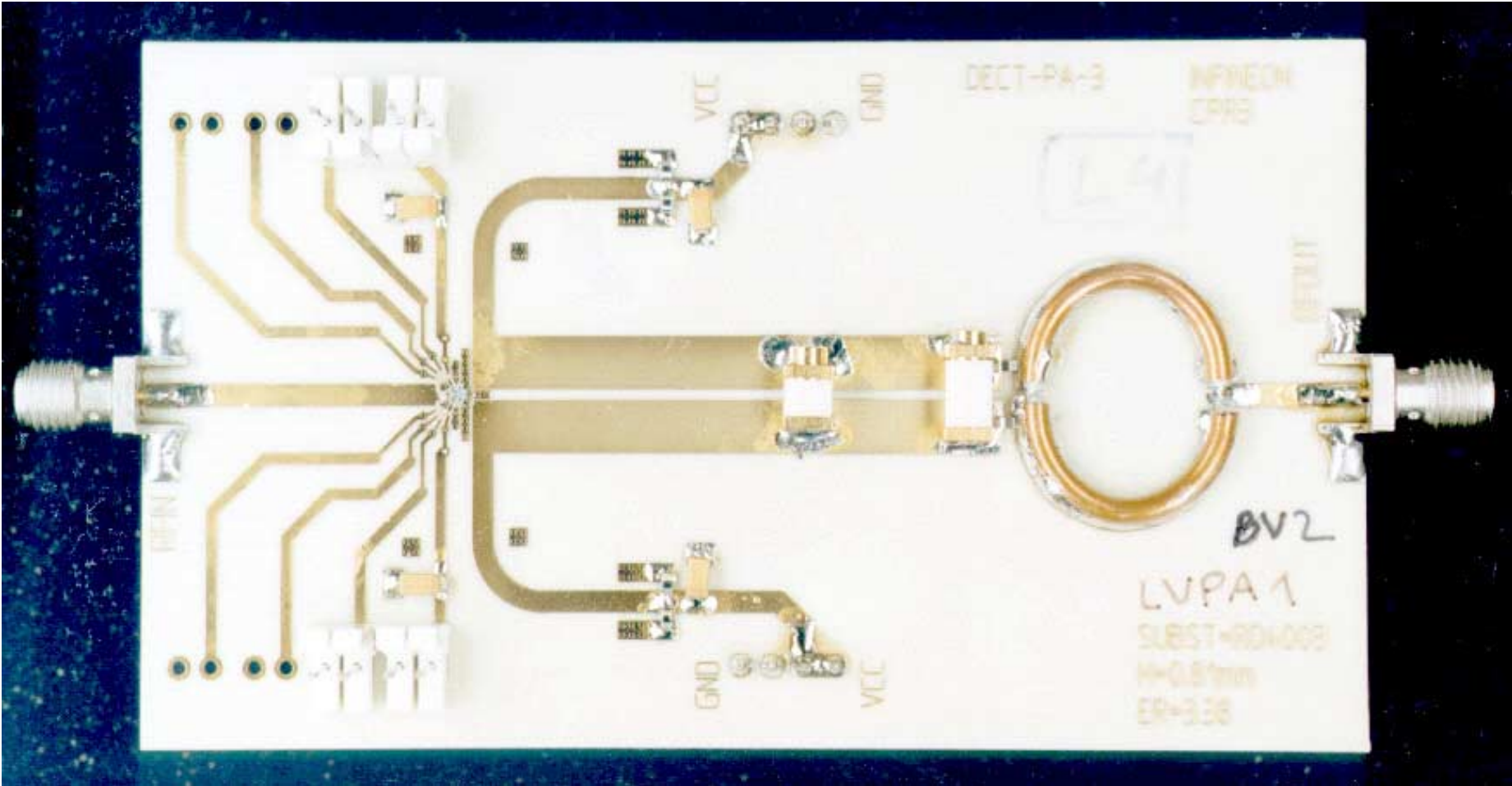
Chip Micrograph (Size 1.17 x 0.97 mm²)



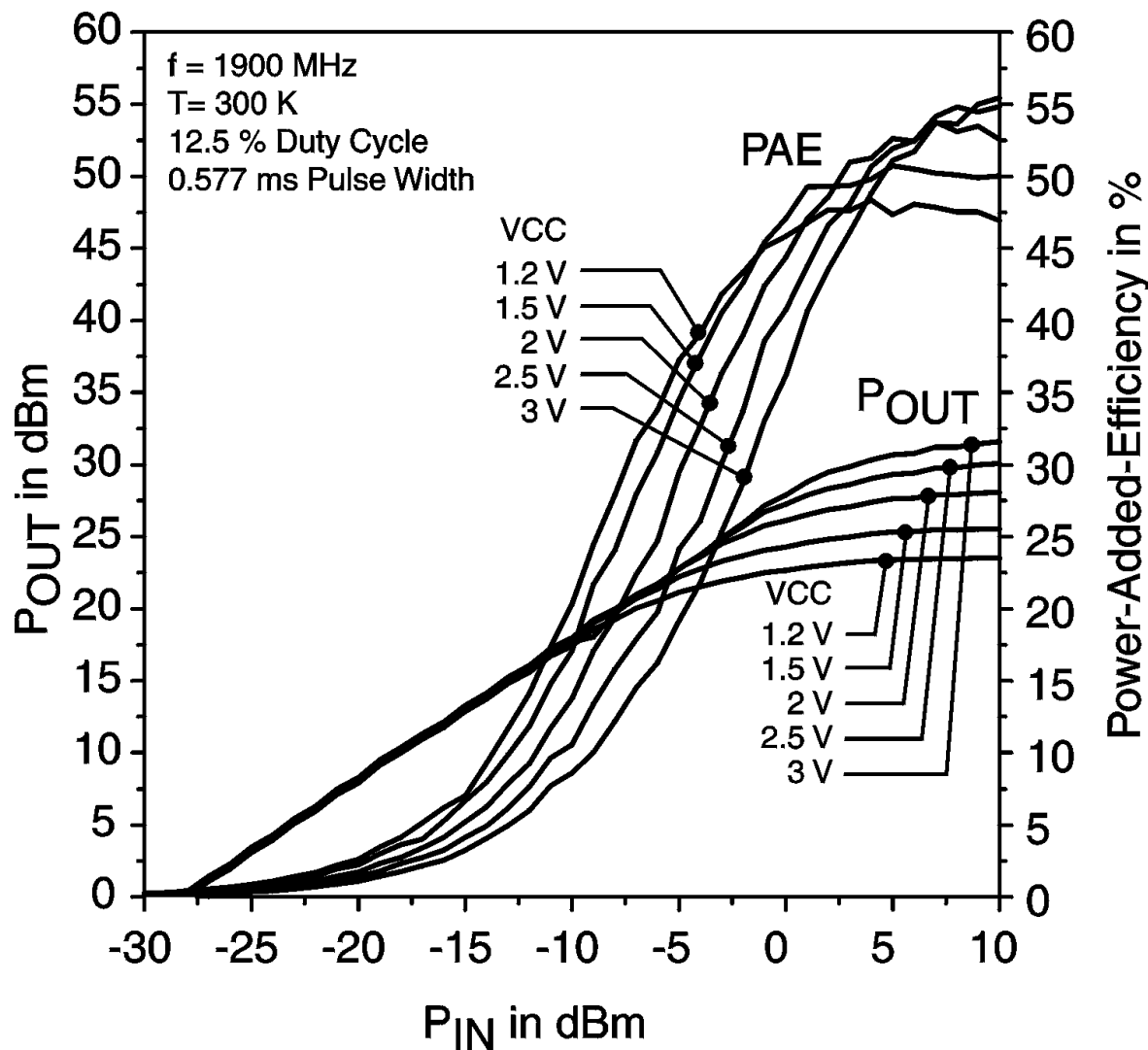
2 GHz Test Circuit



2 GHz Test Board



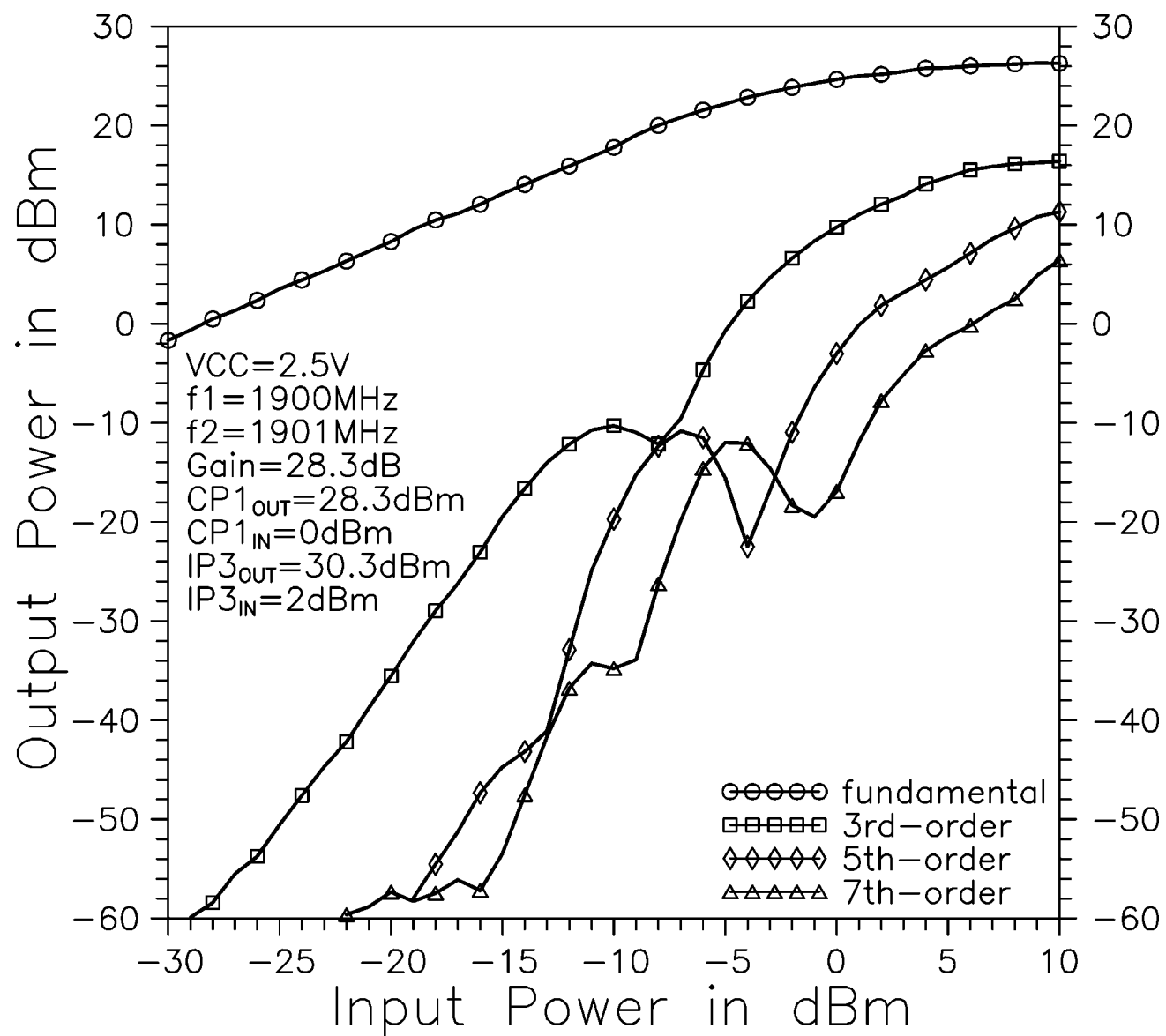
Power Transfer Characteristic and PAE



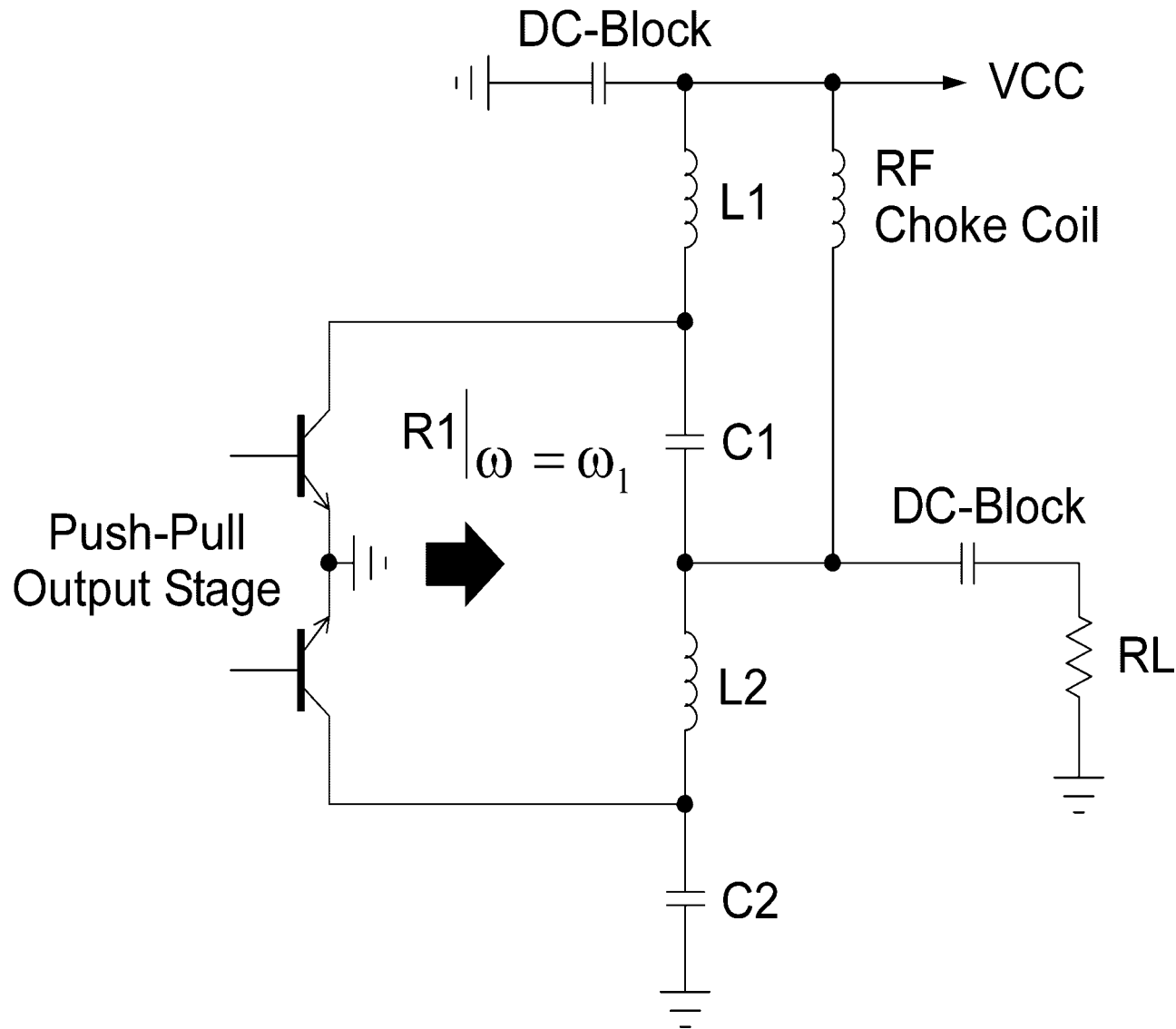
Measurement Data:
($f=1.9\text{GHz}$, $P_{IN}=10\text{dBm}$)

VCC	P _{OUT}	PAE
1.2 V	0.22 W	47 %
1.5 V	0.35 W	50 %
2.0 V	0.63 W	52 %
2.5 V	1 W	55 %
3.0 V	1.4 W	55 %

Intermodulation Characteristic



Application Circuit: Lumped LC-Balun



Bridge Impedance:

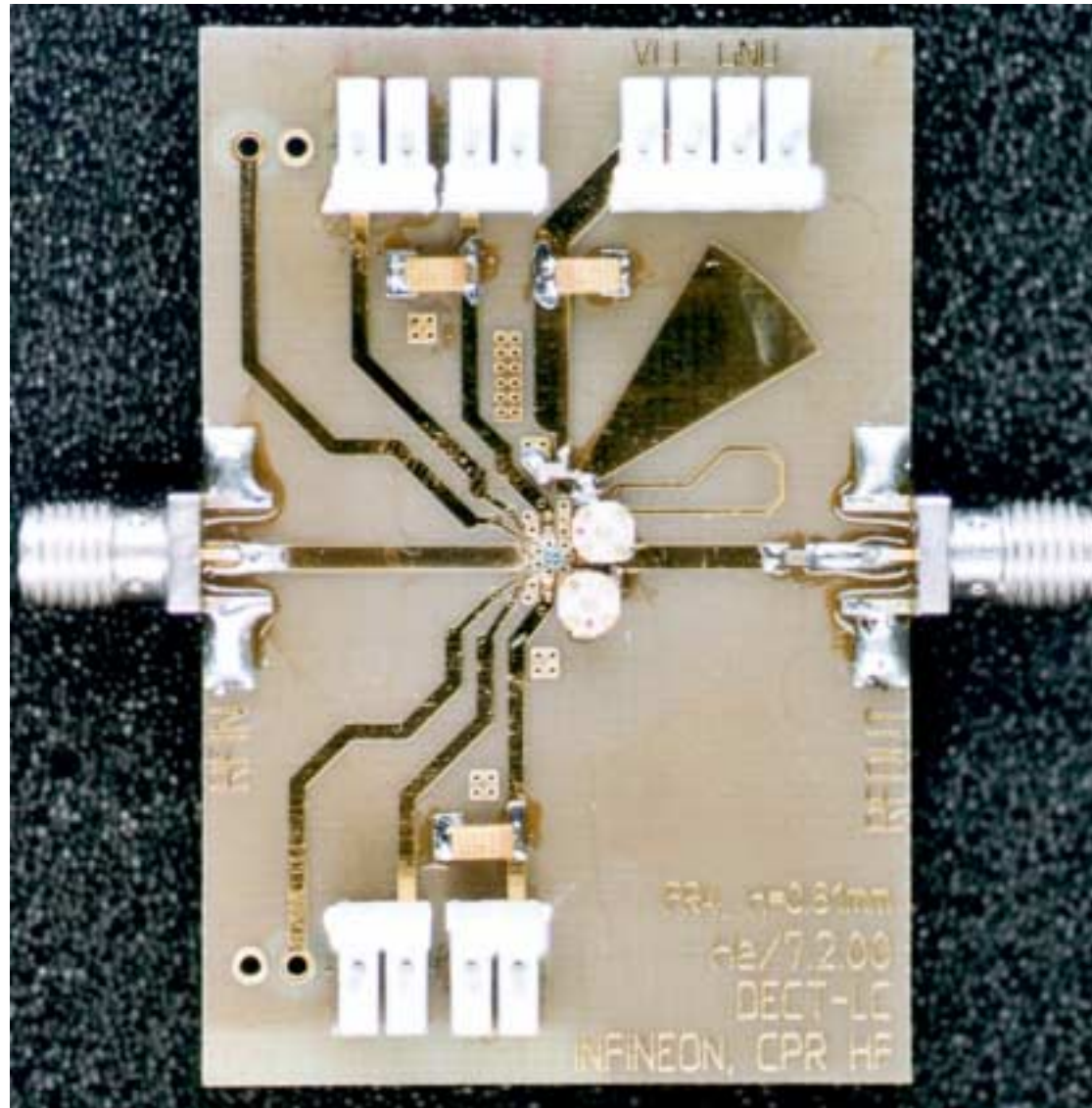
$$Z_1 = \sqrt{R_1 \cdot R_L}$$

Design:

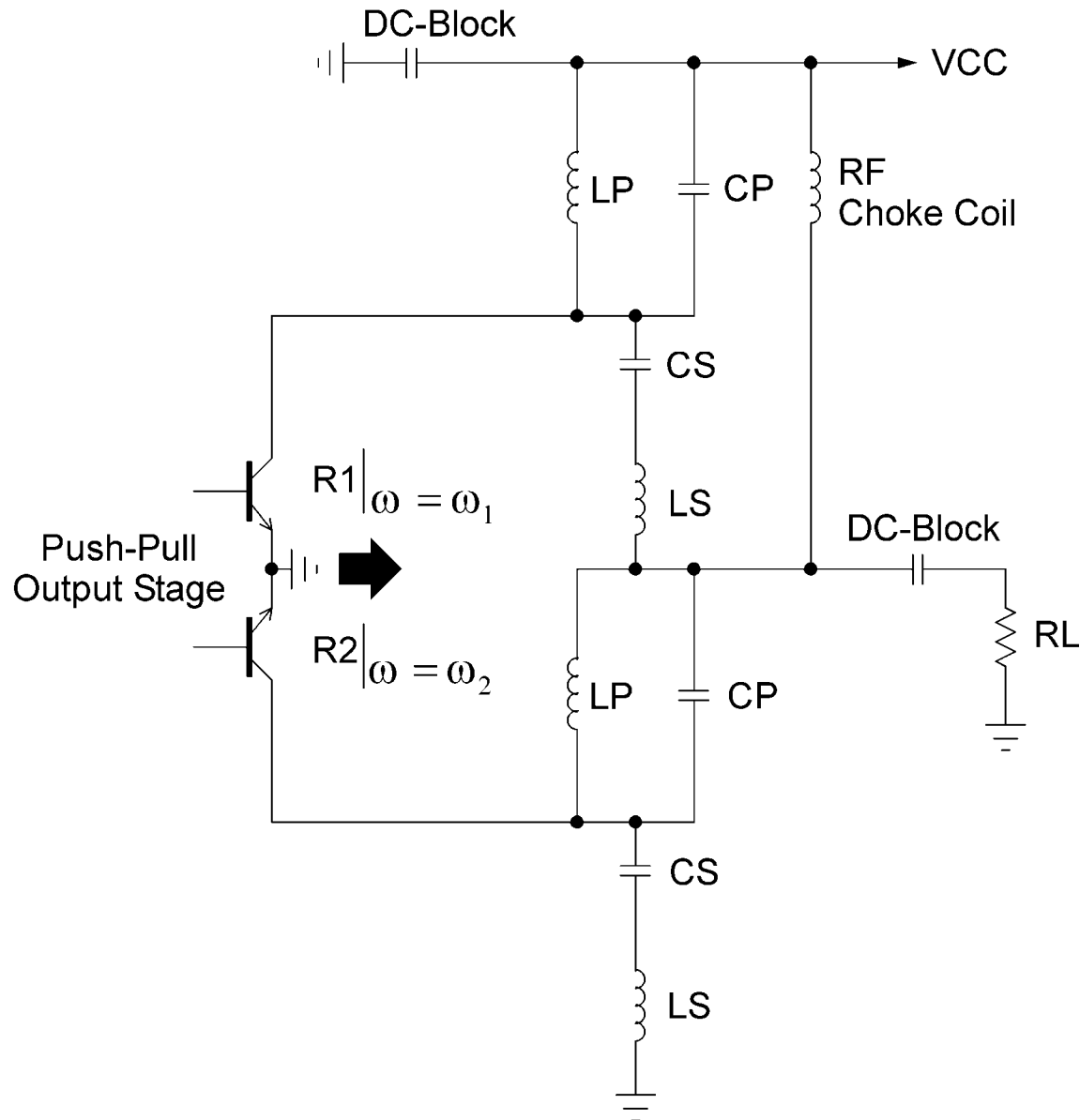
$$L_1 = L_2 = \frac{Z_1}{\omega_1}$$

$$C_1 = C_2 = \frac{1}{\omega_1 \cdot Z_1}$$

Application Board: Lumped LC Balun



Lumped Dual Band LC-Balun



Bridge Impedances:

$$Z_1 = \sqrt{R_1 \cdot R_L}$$

$$Z_2 = \sqrt{R_2 \cdot R_L}$$

Design:

$$L_S = \frac{\omega_1 \cdot Z_1 + \omega_2 \cdot Z_2}{\omega_2^2 - \omega_1^2}$$

$$C_S = \frac{\frac{\omega_2 - \omega_1}{\omega_1 \omega_2}}{\omega_1 \cdot Z_2 + \omega_2 \cdot Z_1}$$

$$L_P = \frac{\left(\frac{\omega_2 - \omega_1}{\omega_1 \omega_2} \right) \cdot Z_1 \cdot Z_2}{\omega_1 \cdot Z_1 + \omega_2 \cdot Z_2}$$

$$C_P = \frac{\omega_1 \cdot Z_2 + \omega_2 \cdot Z_1}{(\omega_2^2 - \omega_1^2) \cdot Z_1 \cdot Z_2}$$

$$\omega_2 > \omega_1$$

Performance Summary

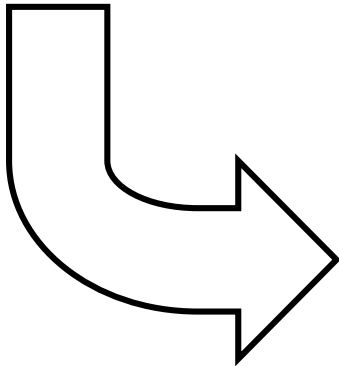
Operating Frequency	1800 - 2000	MHz
Supply Voltage	1.2 - 3	V
Maximum Output Power (at 1.2 V / 3 V and 1900 MHz, $P_{in} = 10$ dBm)	0.22 / 1.4	W
Maximum PAE (at 0.22 W / 1.4 W and 1900 MHz)	47 / 55	%
Output-Stage Collector Efficiency (at 0.22 W / 1.4 W and 1900 MHz)	61 / 67	%
Small-signal Gain (at 1900 MHz)	28	dB
Technology	0.5 μm , 50 GHz f_T Si-Bipolar	

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- ▶ Conclusion

Challenges

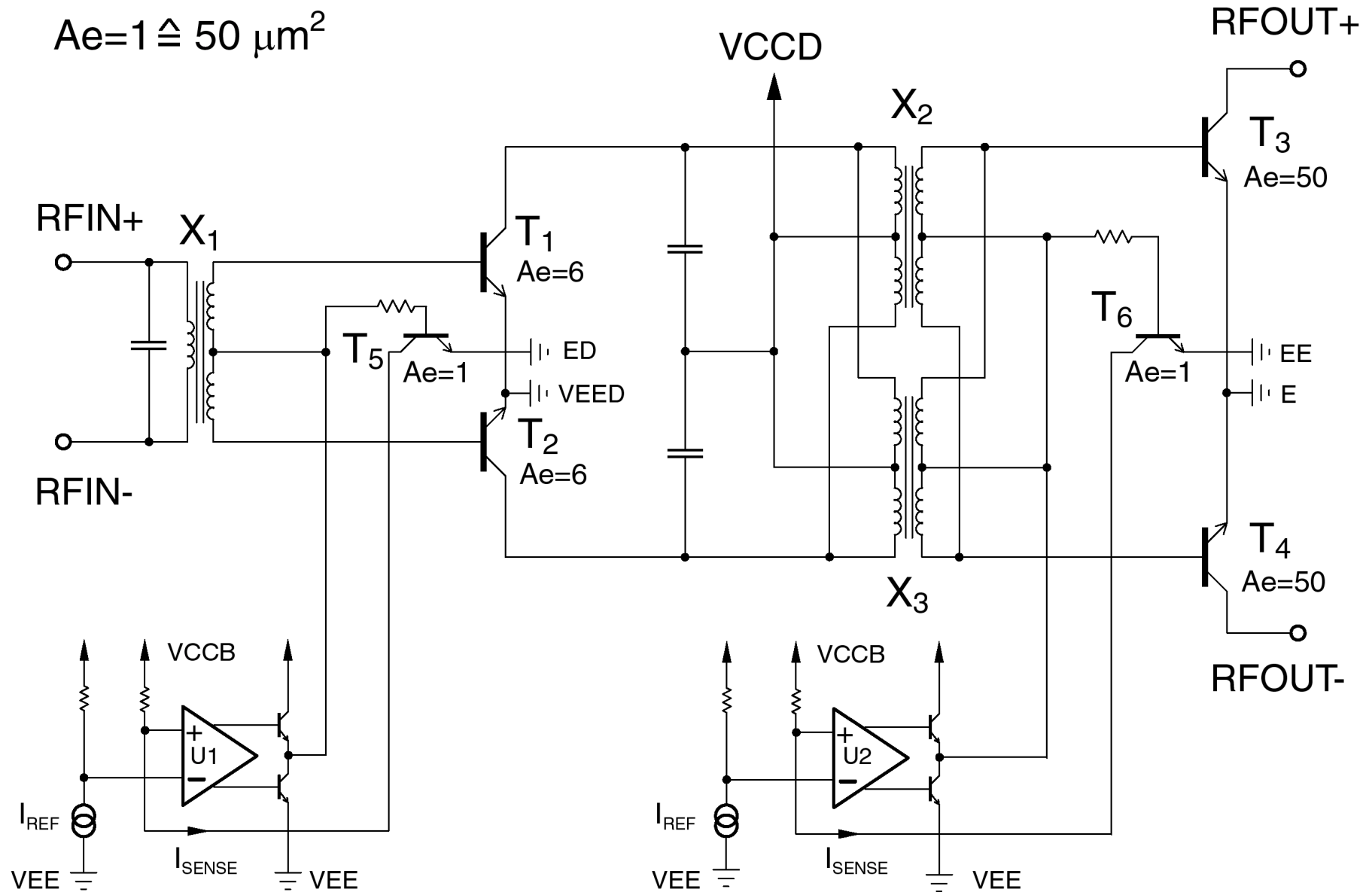
- Output Power > 2.5 W at 900 MHz and 2.8 V
- Efficiency > 50 %
- Power Supply Range 2.8 V to 4.5 V
- Standard 0.8 μm Si-Bipolar Technology, $f_T = 25$ GHz



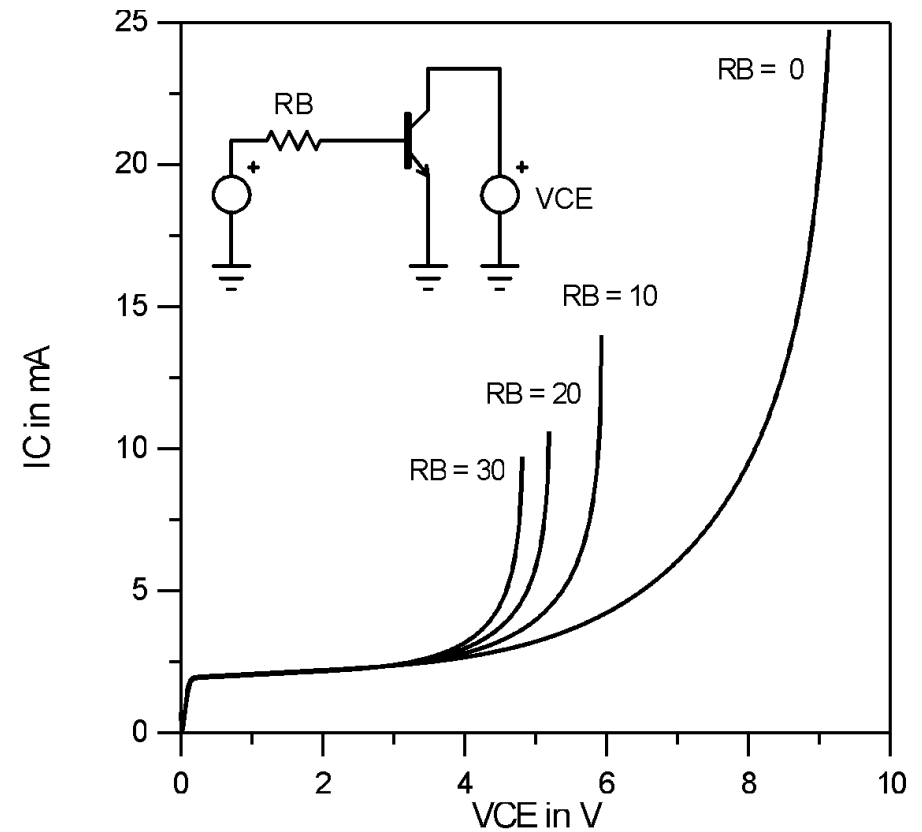
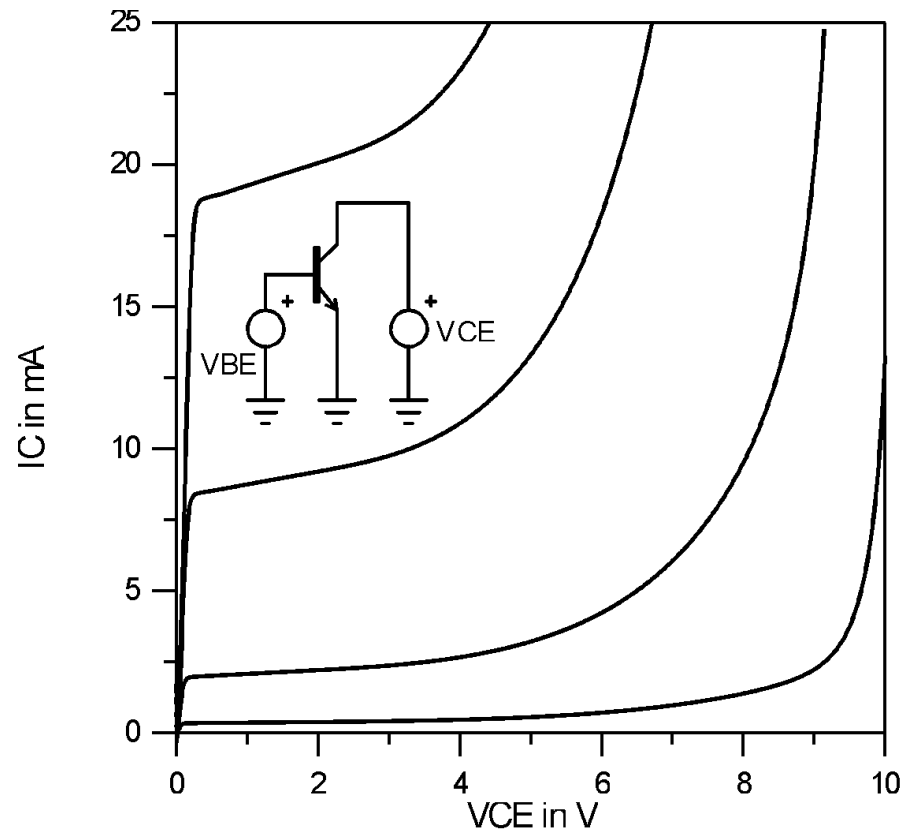
Approaches Used

- ▶ Push-Pull Type Circuit
- ▶ 900 MHz High Performance Transformers
- ▶ Closed Loop Bias Circuit

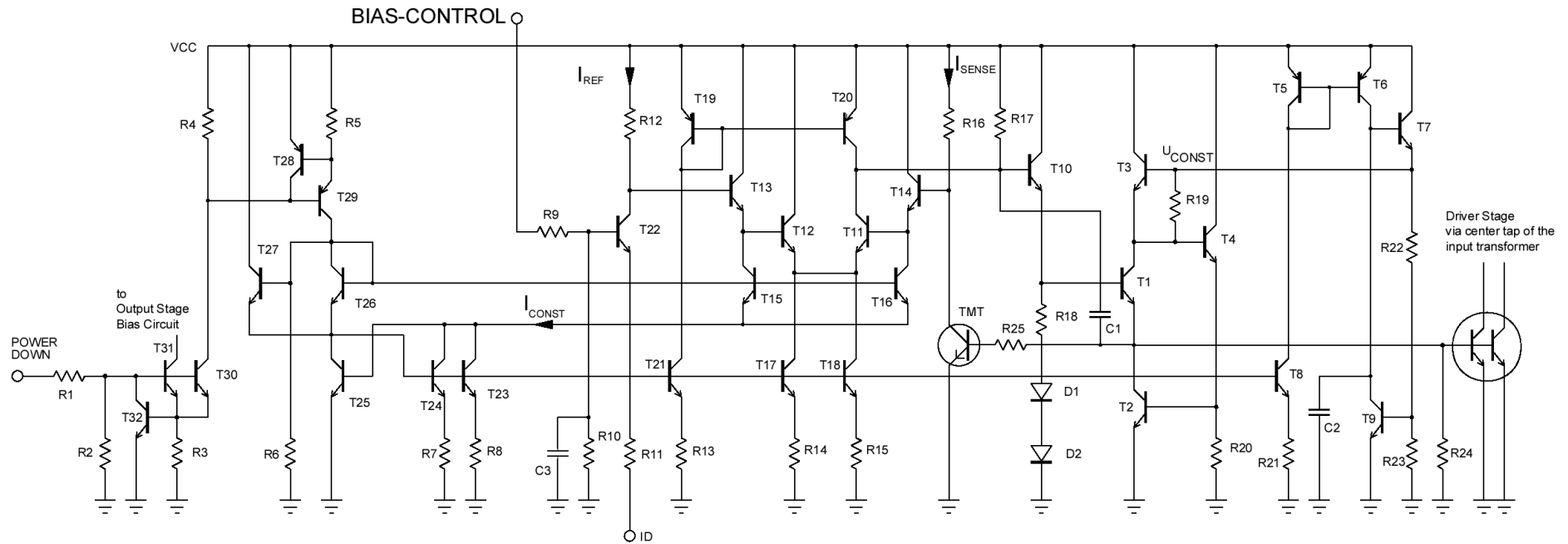
900 MHz PA Circuit Diagram



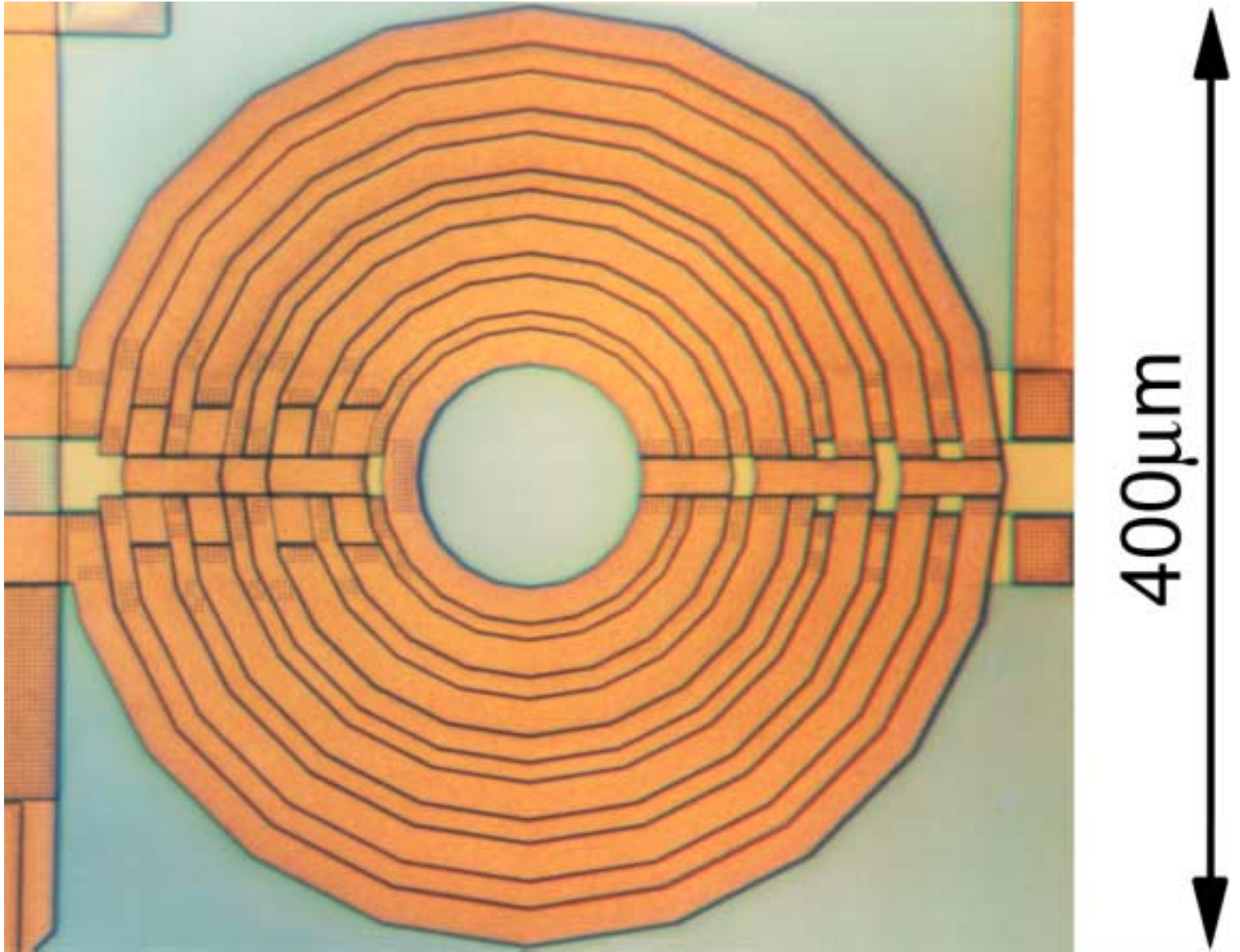
BJT Breakdown Characteristics



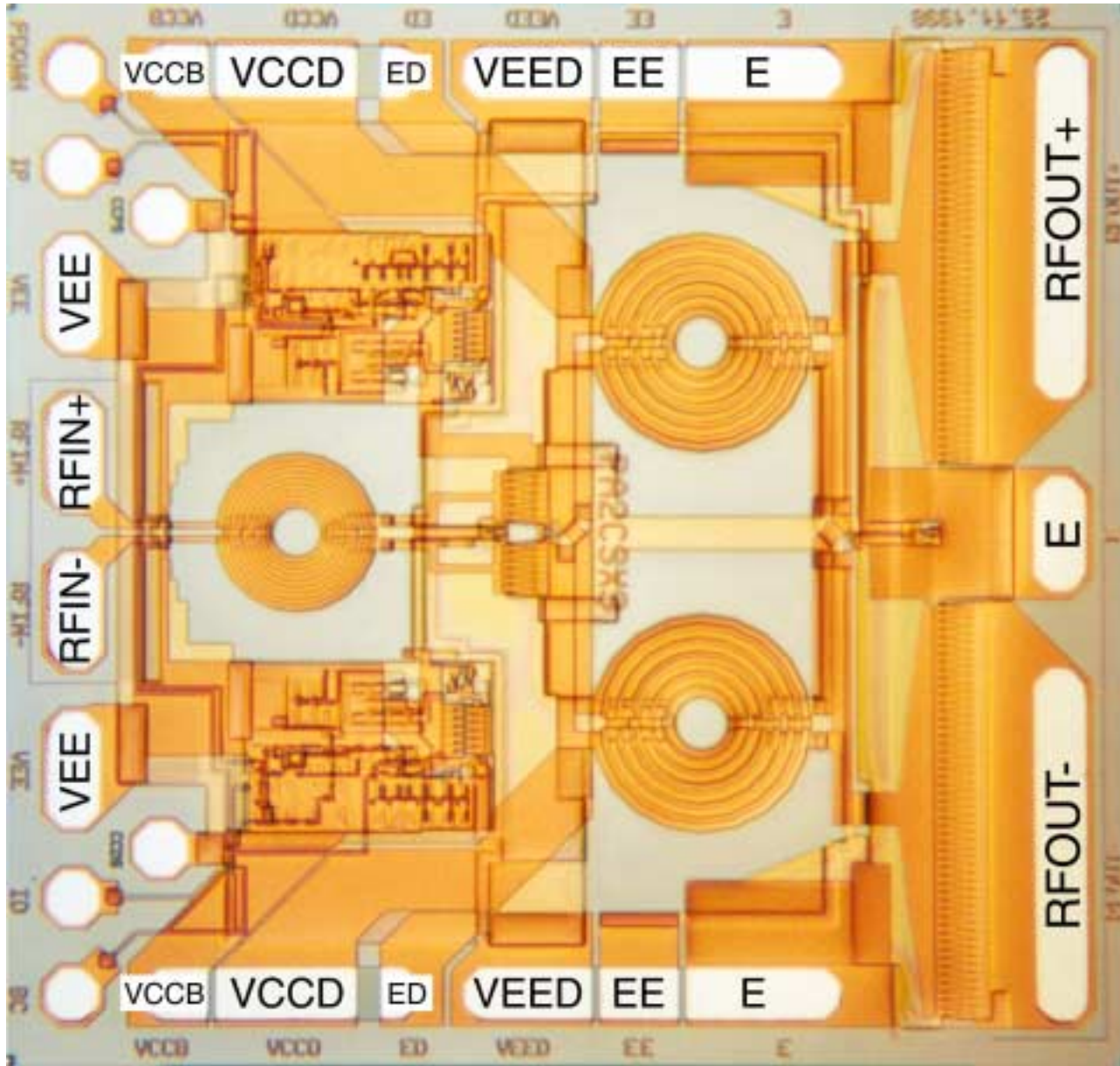
Bias Opamp Circuit Diagram



900 MHz Transformer Photograph



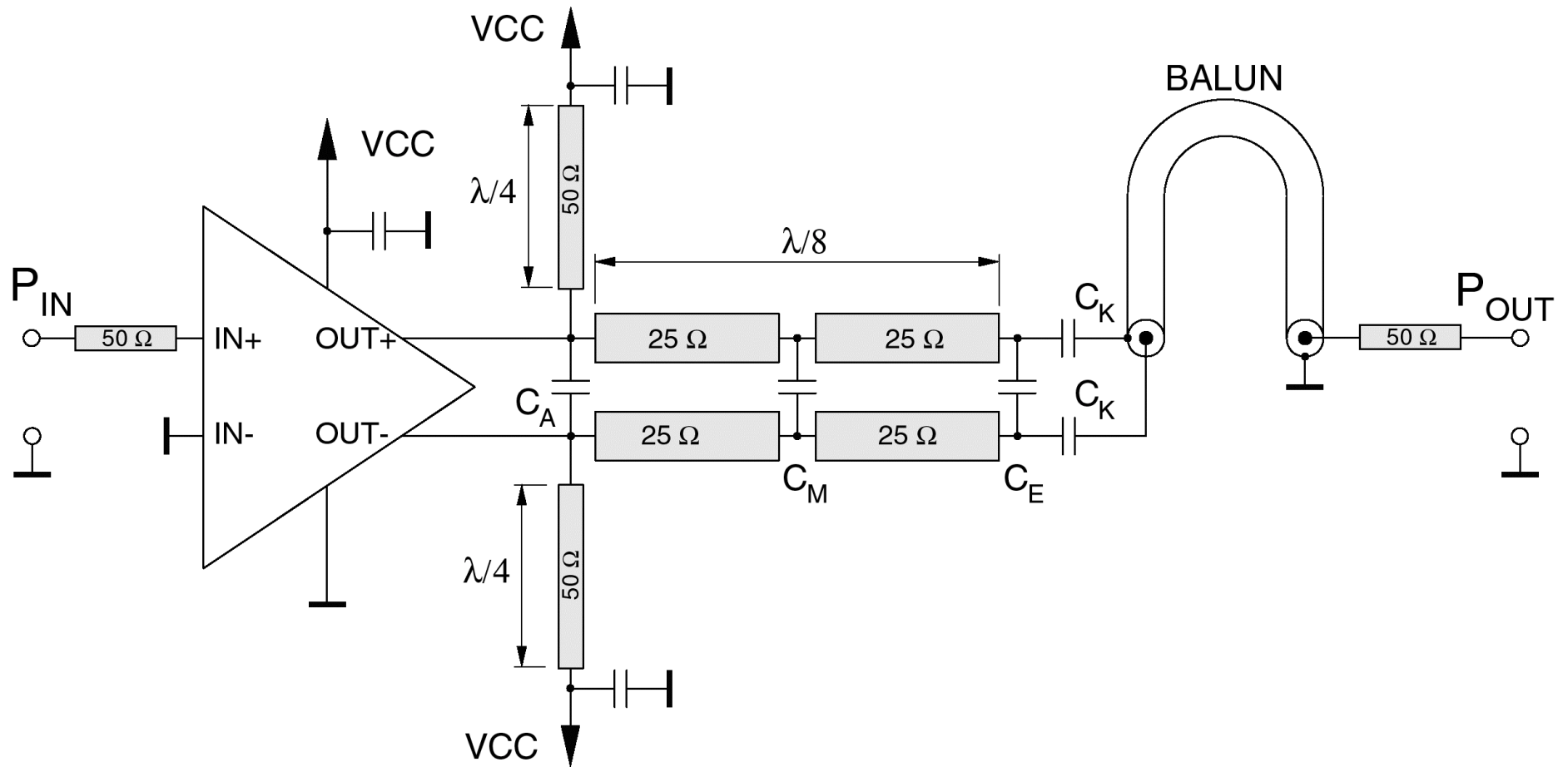
Chip Photograph



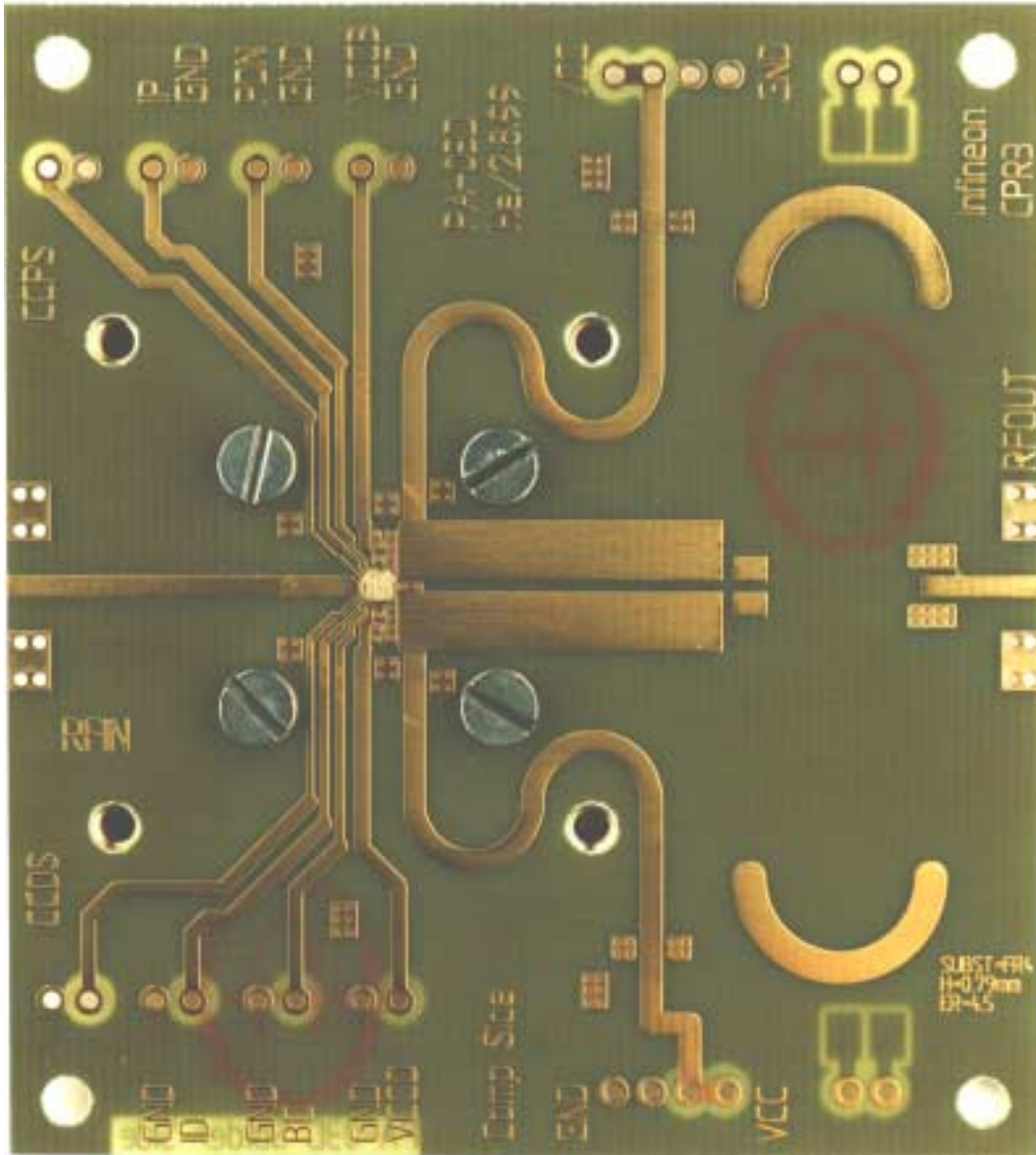
2mm



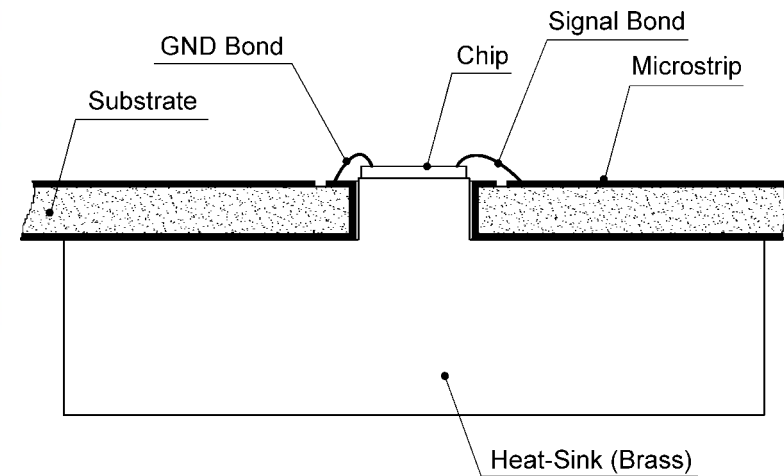
900 MHz Test Circuit



Power Amplifier Test Board

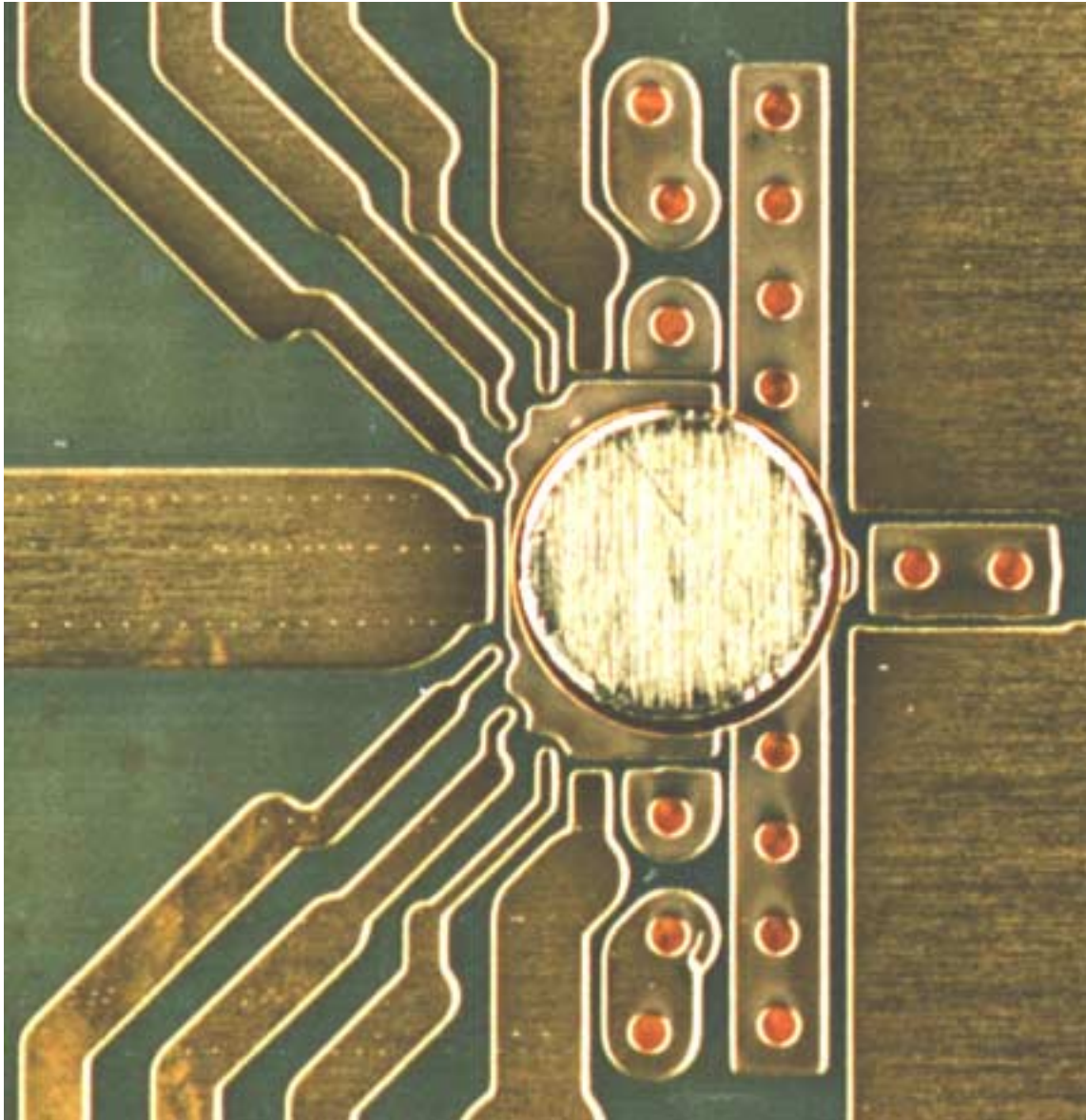


Cross Section

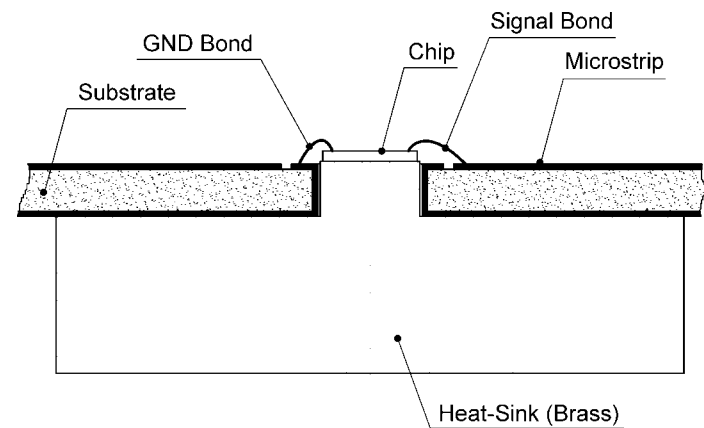


Power Amplifier Test Printed Circuit Board
(FR4, 70 x 78 mm²)

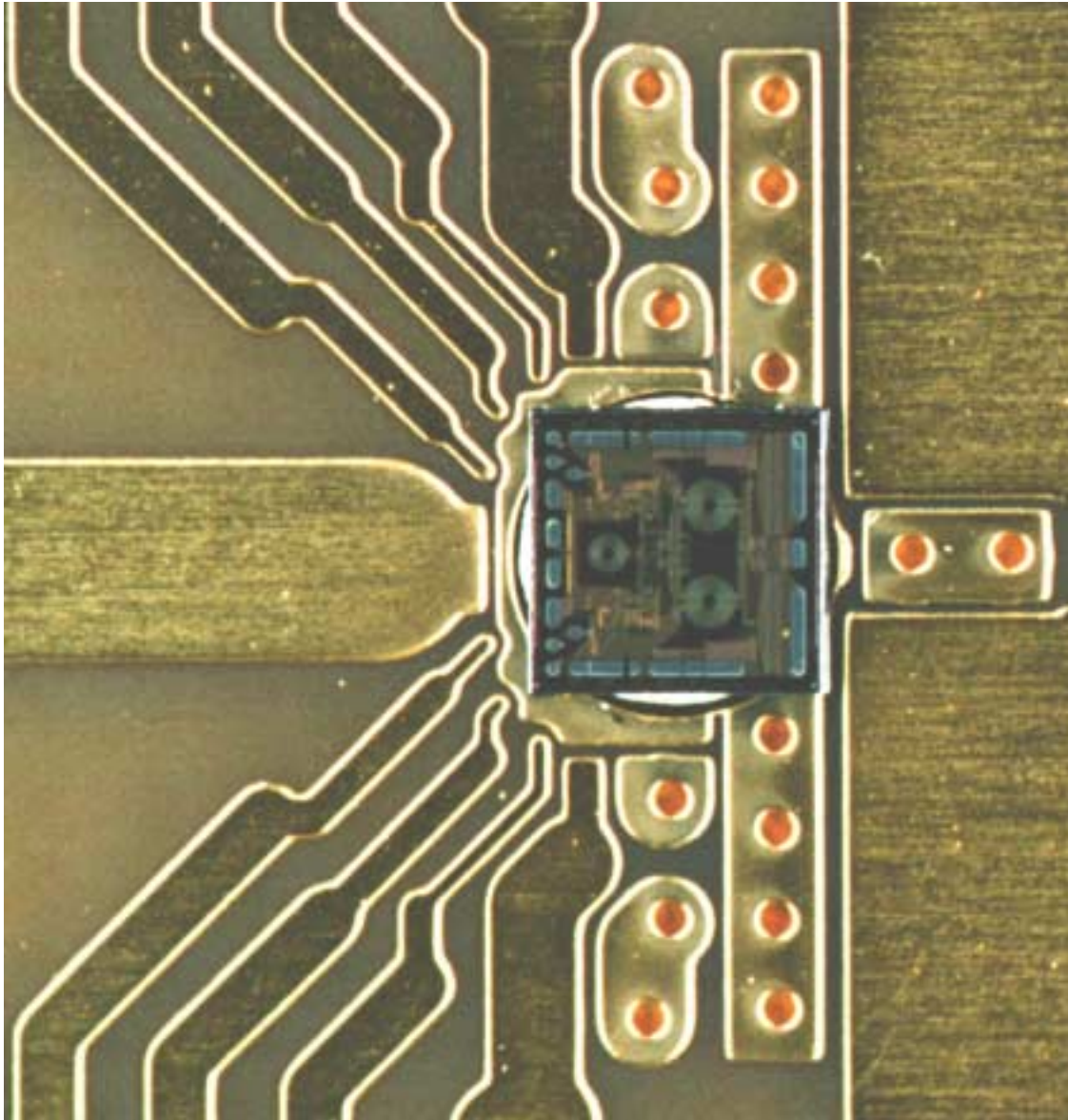
Test Circuit Detail View (Heat-Slug)



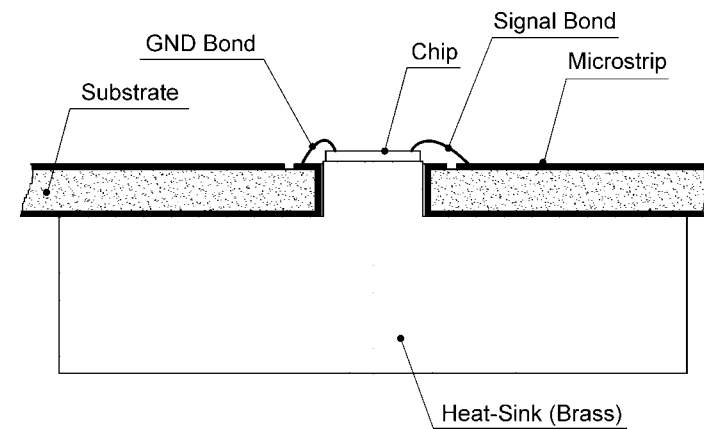
Cross Section



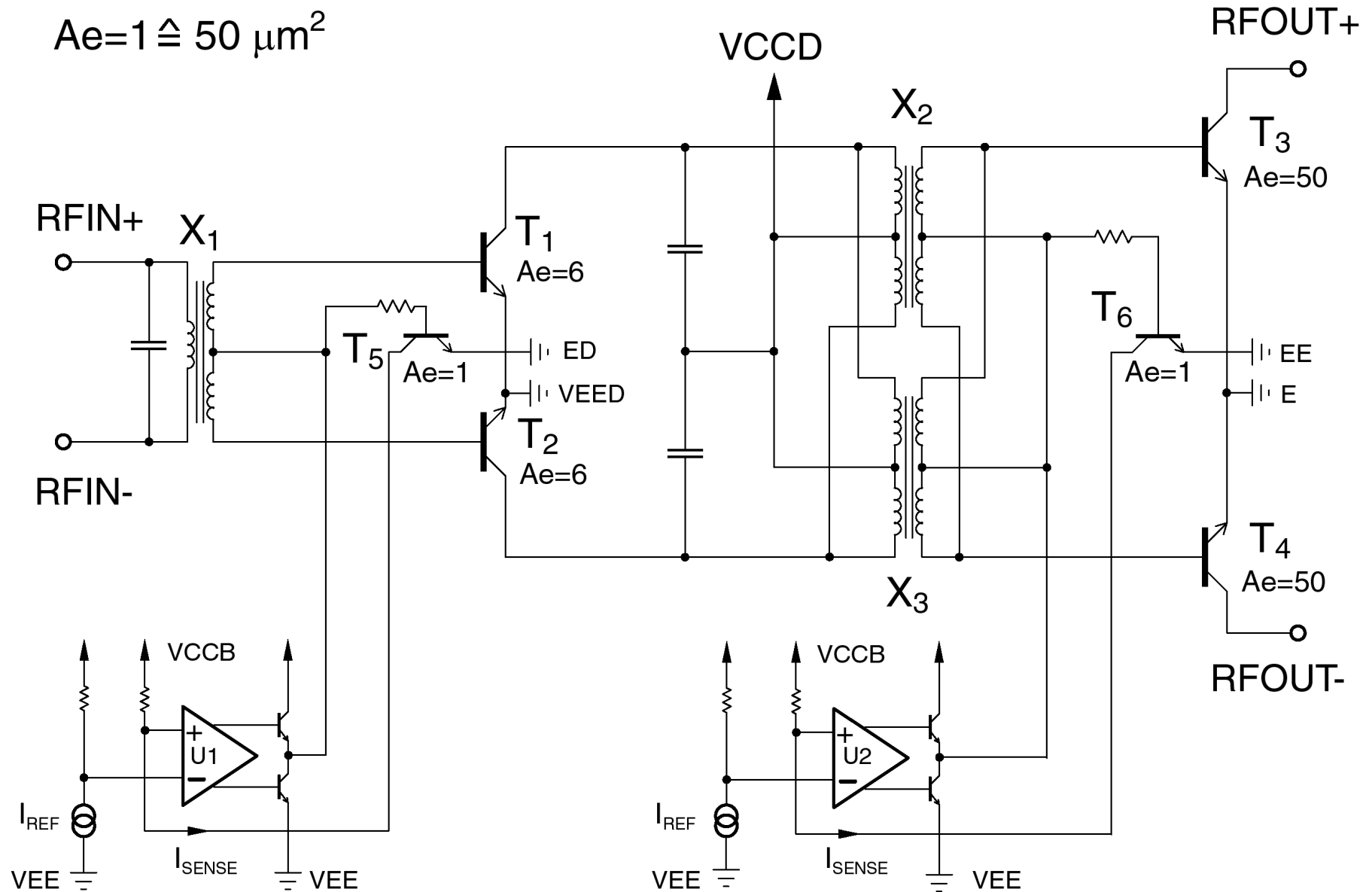
Test Circuit Detail View (Heat-Slug)



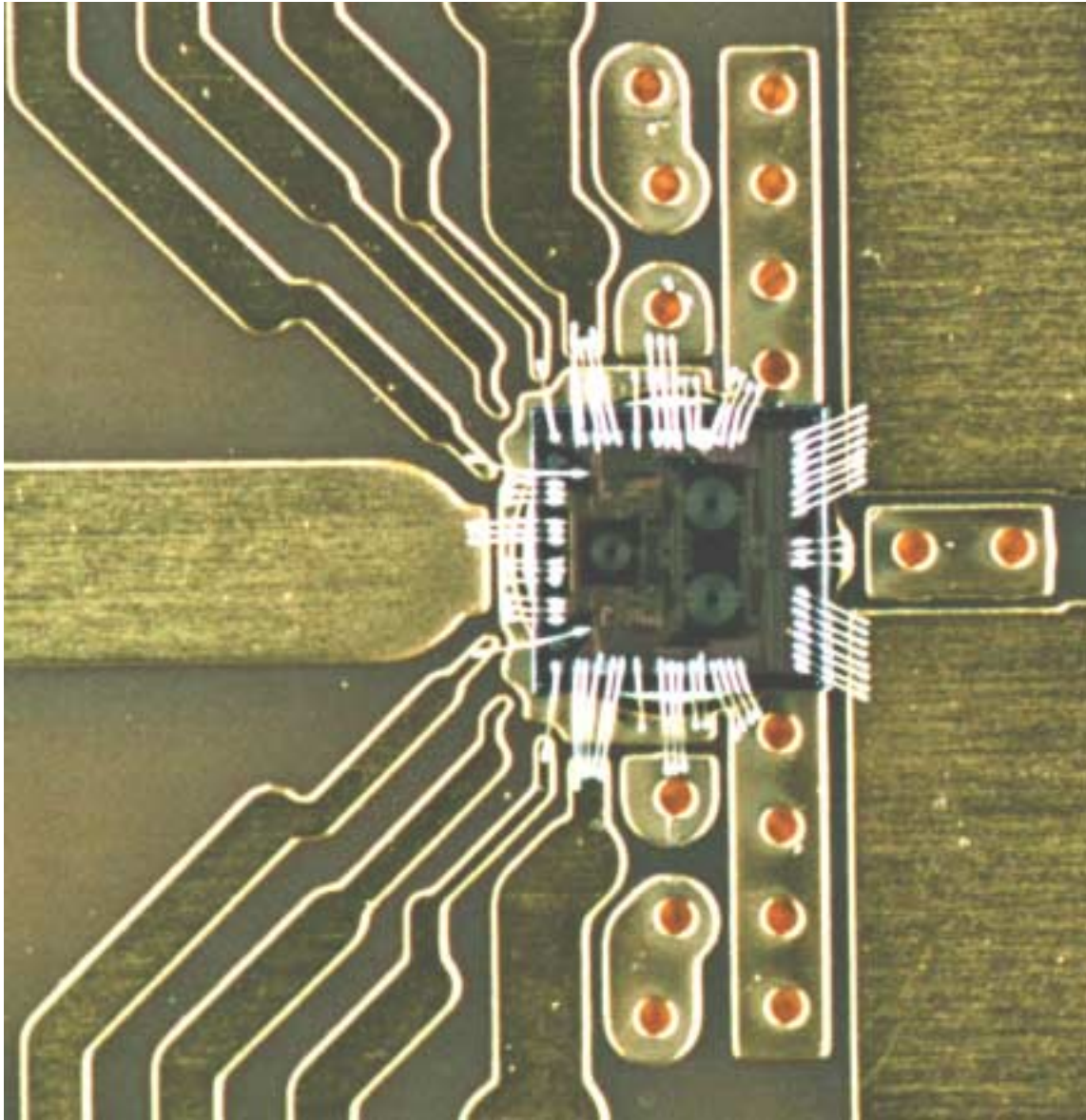
Cross Section



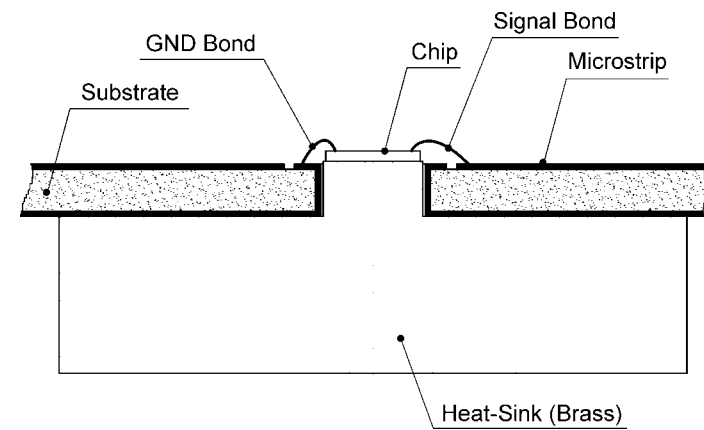
900 MHz PA Circuit Diagram



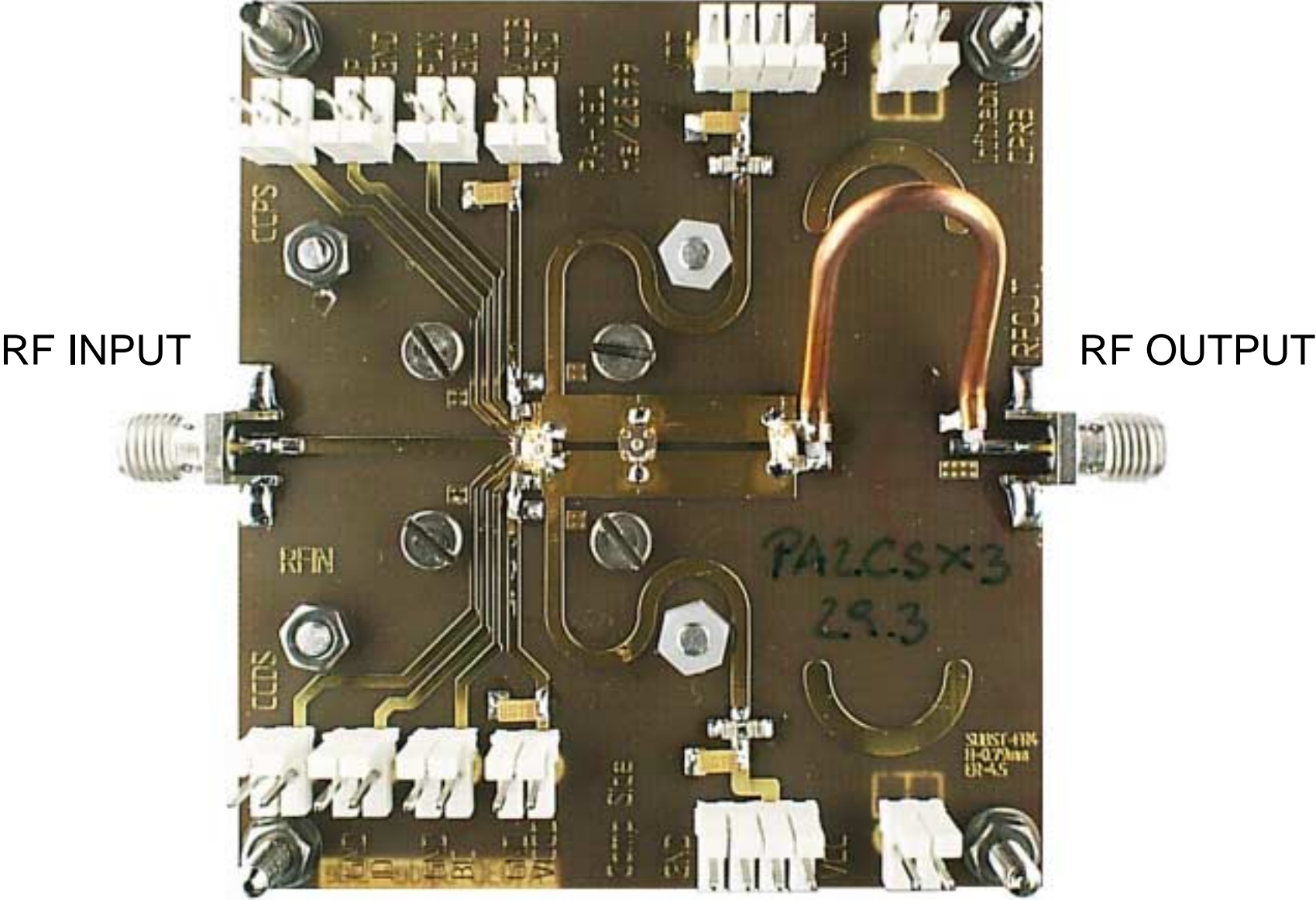
Test Circuit Detail View (Heat-Slug)



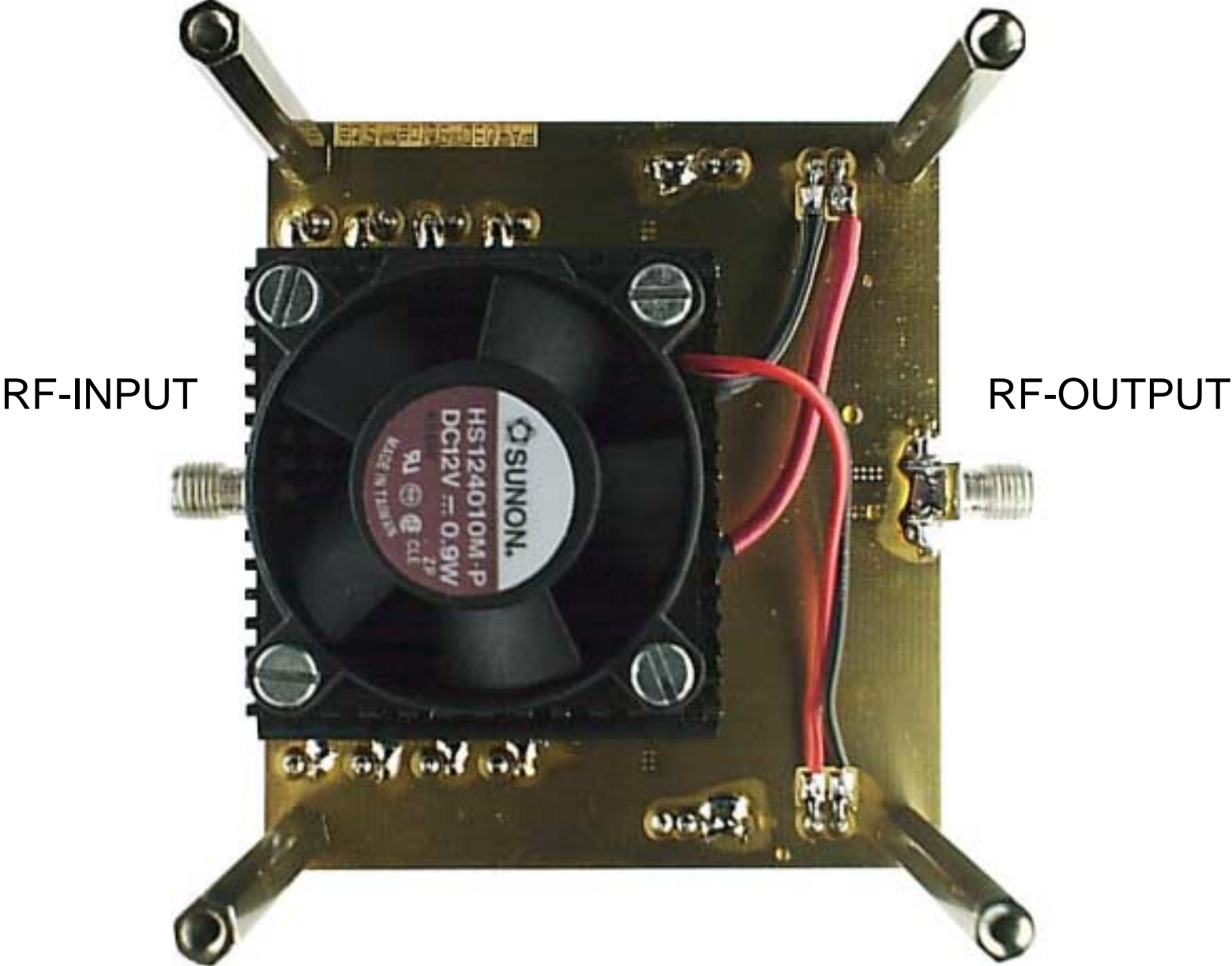
Cross Section



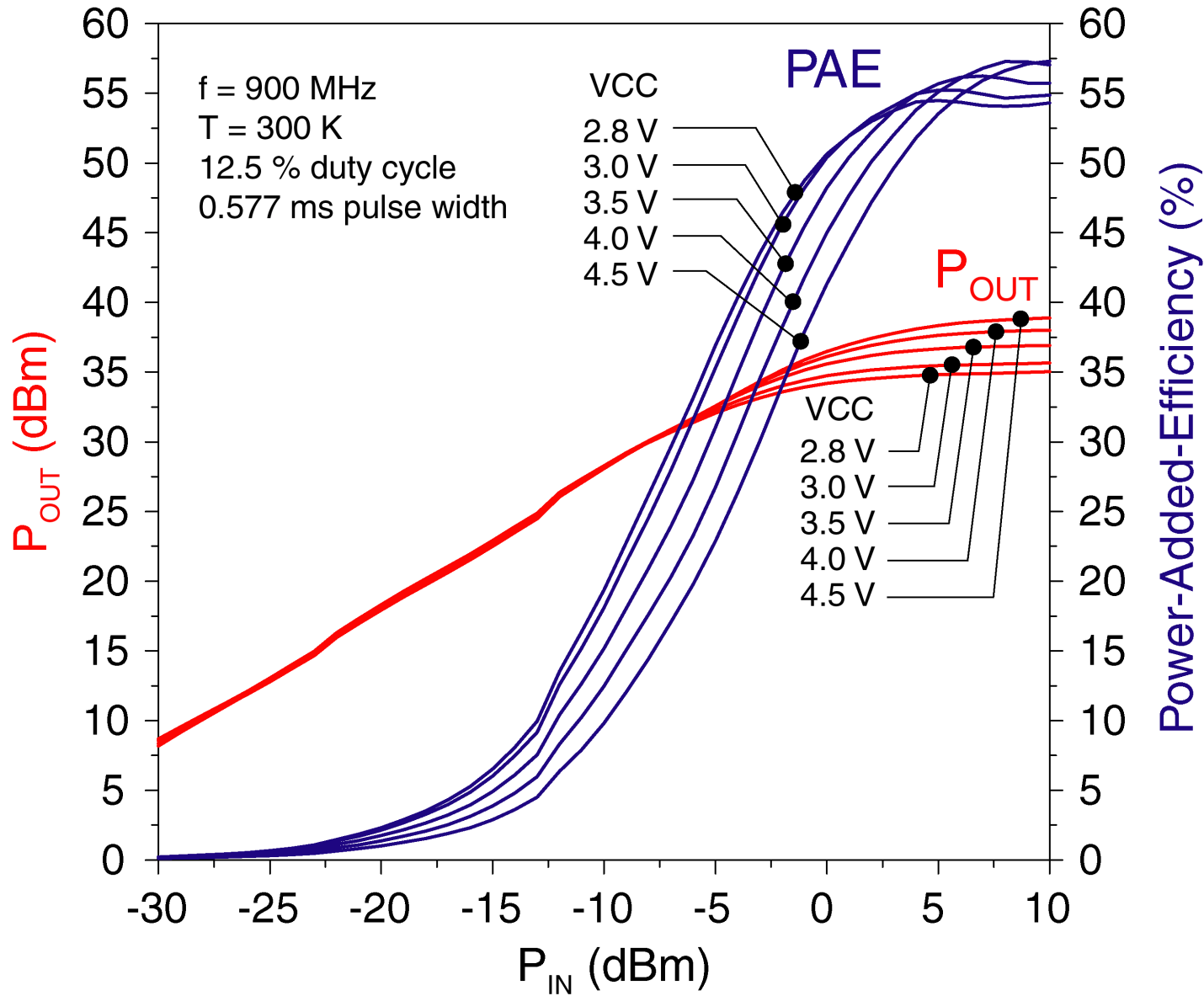
Power Amplifier Test Board Top-View



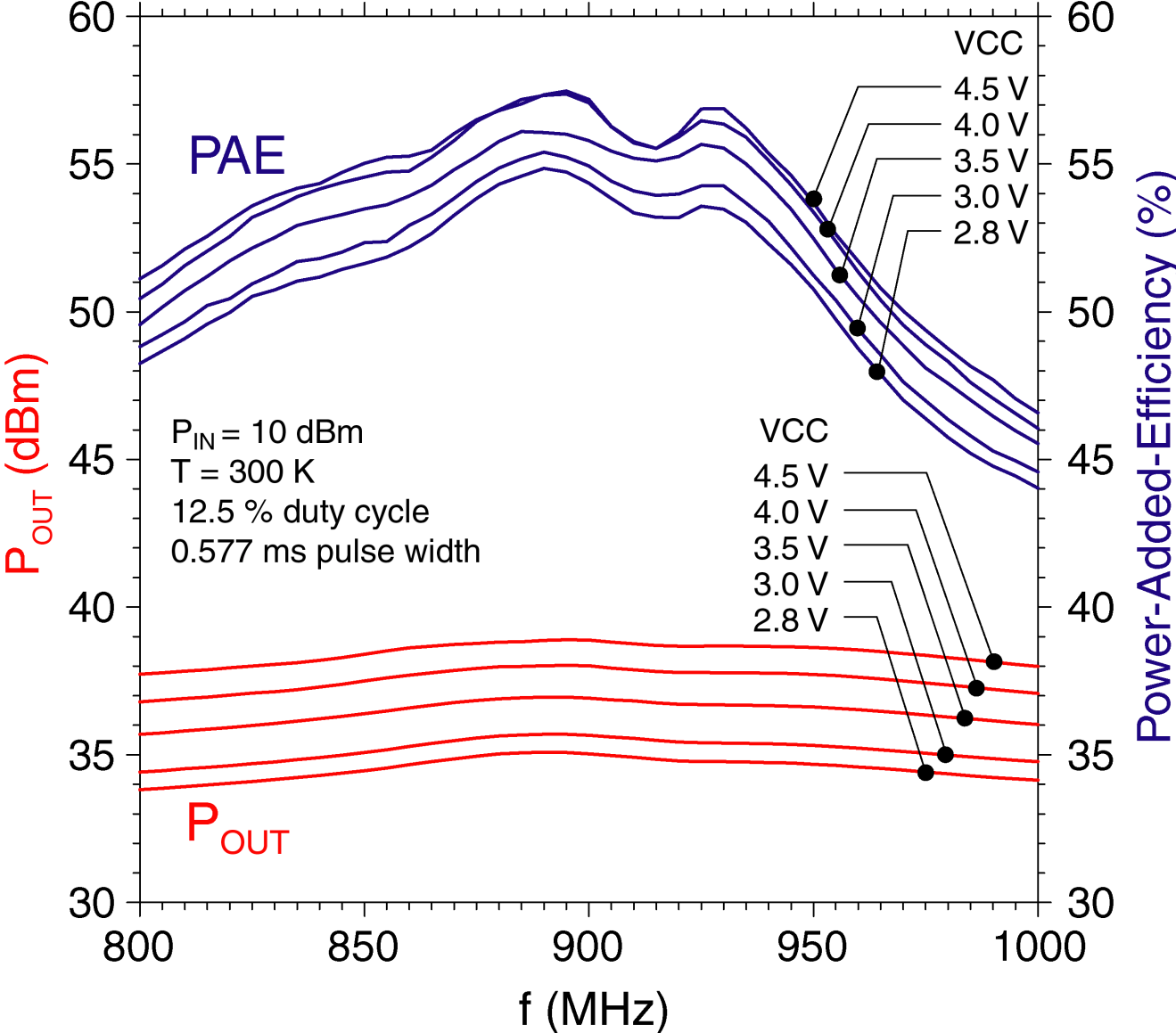
Power Amplifier Test Board Bottom-View



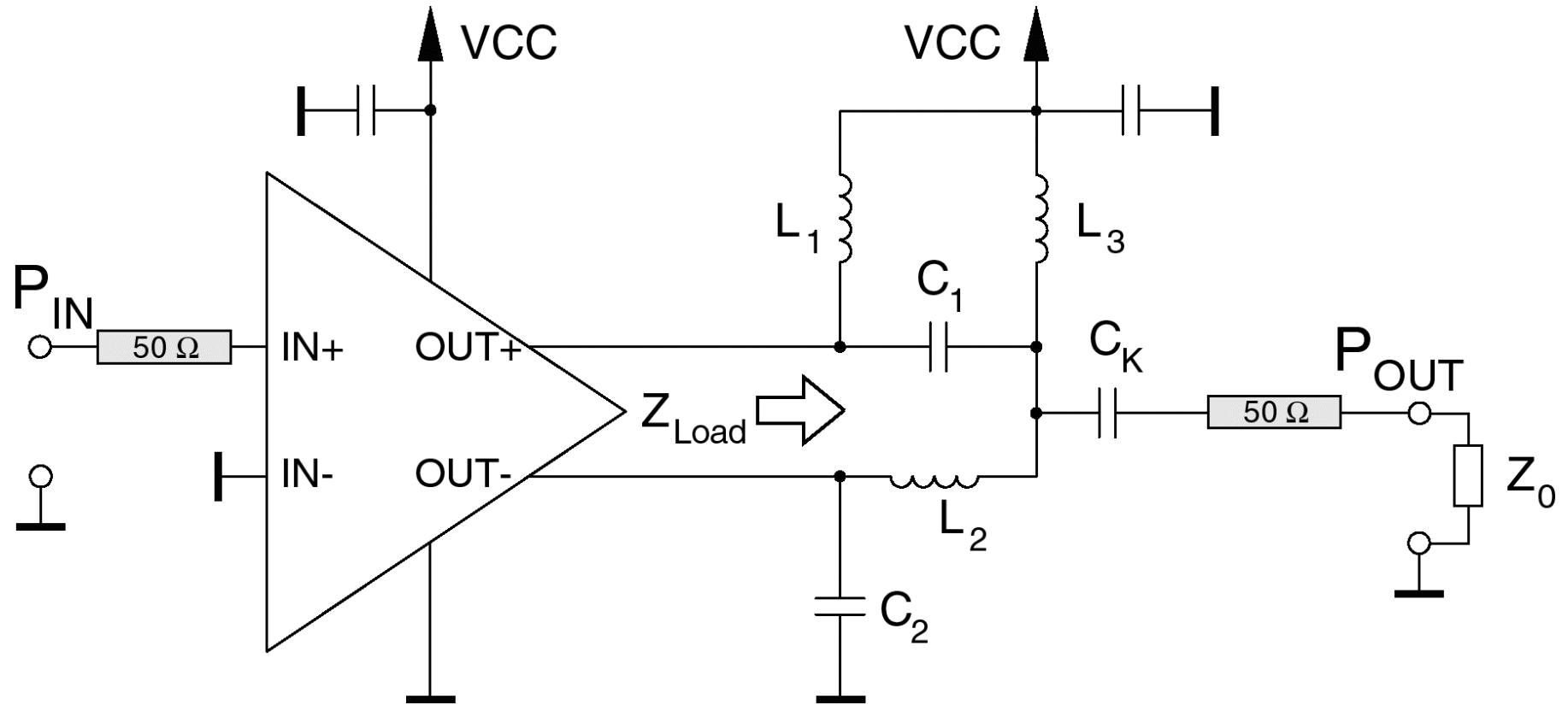
Power Transfer Characteristic (Test Board)



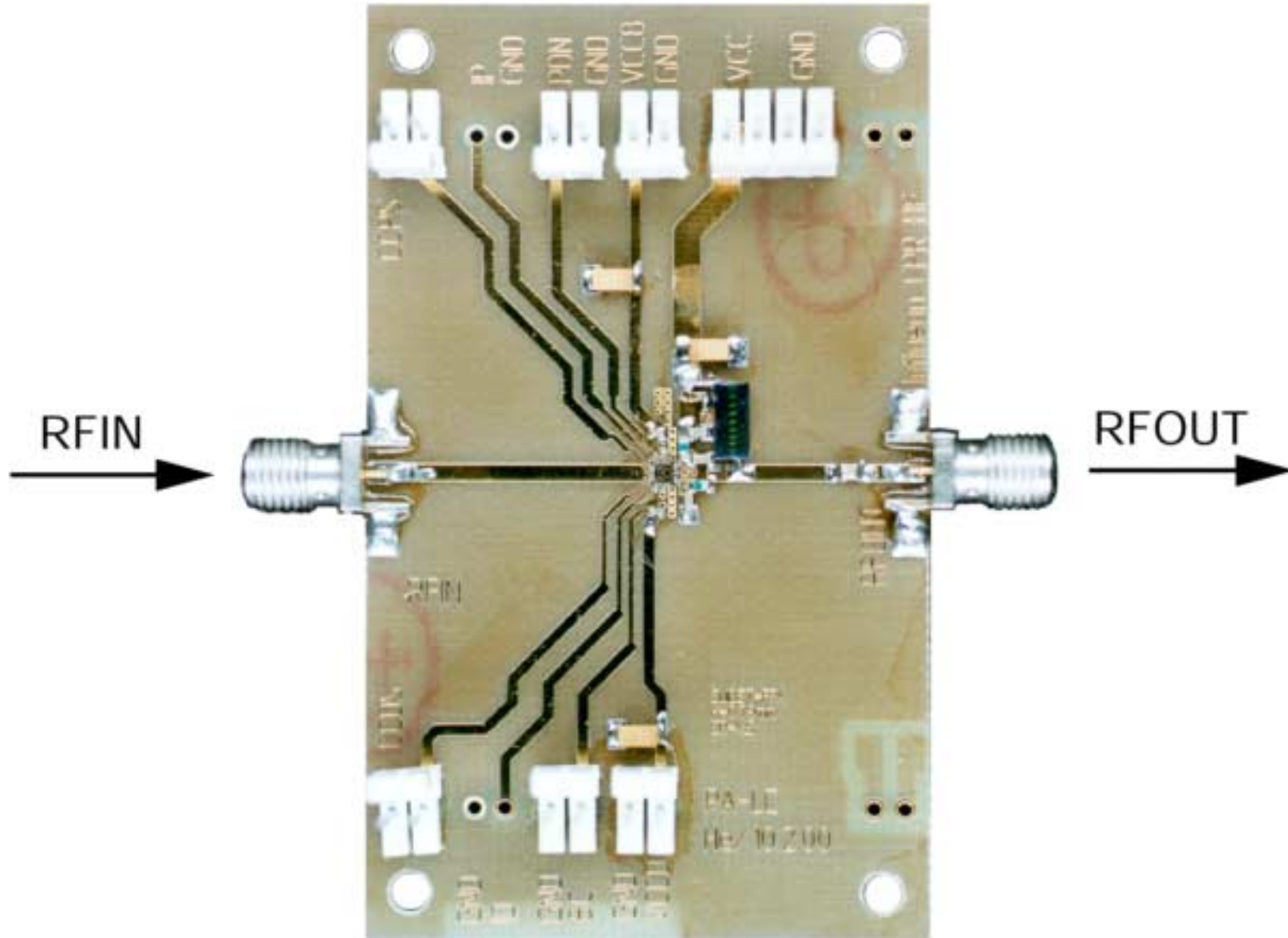
Frequency Response (Test Board)



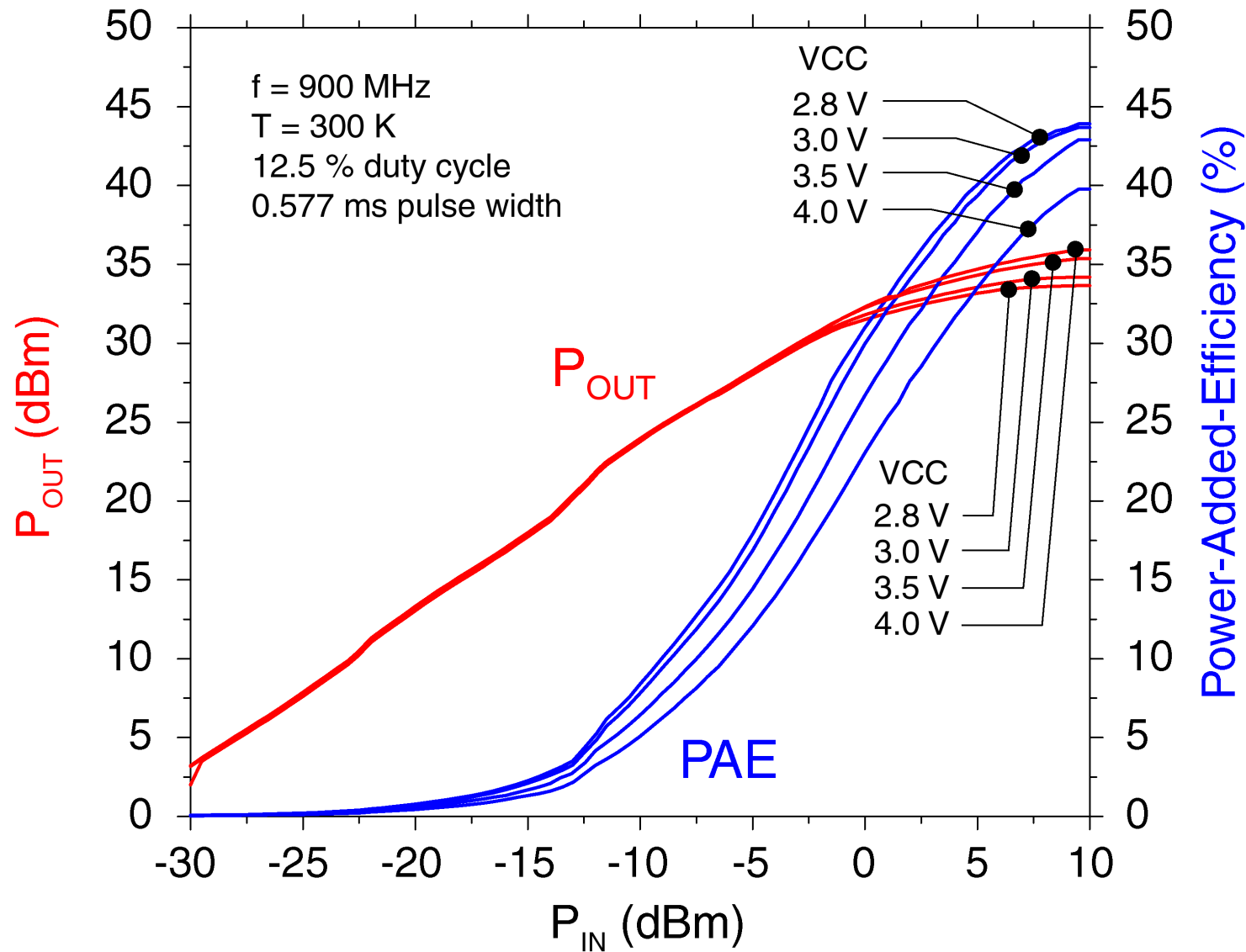
Application Circuit



Application Board



Power Transfer Characteristic and PAE (Application Board)



Performance Summary

Operating Frequency	800 - 1000	MHz
Supply Voltage	2.8 - 4.5	V
Maximum Output Power (at 2.8 V / 4.5 V and 900 MHz, Pin = 10 dBm)	3.2 / 7.7	W
Maximum PAE (at 3.2 W / 7.7 W and 900 MHz)	54 / 57	%
Output-Stage Collector Efficiency (at 3.2 W / 7.7 W and 900 MHz)	66 / 68	%
Input VSWR (at 900 MHz)	1.7	
Small-signal Gain (at 900 MHz)	38	dB
Technology	0.8 μm , 25 GHz f_T Si-Bipolar	

Conclusion

- ▶ High performance on-chip transformer

- ▶ Integrated push-pull type PAs in Si-bipolar:
 - a) 1 W, 1.9 GHz, 55 % PAE at 2.5 V
 - b) 3.2 W, 900 MHz, 54 % PAE at 2.8 V