MONOLITHIC TRANSFORMER-COUPLED RF POWER AMPLIFIERS IN SI-BIPOLAR

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ABSTRACT

Monolithic integrated lumped planar transformers were introduced more than ten years ago. We present a comprehensive review of the electrical characteristics which results in an accurate lumped low-order equivalent model. Amplifiers, mixers and Meissner-type voltage controlled oscillators using monolithic transformers have been published a few years ago. For the first time, integrated transformer-coupled power amplifiers with a high performance up to 2 GHz are demonstrated.
This presentation gives an introduction into monolithic transformer and circuit design of push-pull type power amplifiers. Two designs were realized:
1) A monolithic 2 V, 1 W Si-bipolar power amplifier with 55 % power-added efficiency at 1.9 GHz.
2) A monolithic 2.8 V, 3.2 W Si-bipolar power amplifier with 54 % power-added efficiency at 900 MHz.

1. INTRODUCTION

Transformers have been used in radio frequency (rf) circuits since the early days of telegraphy. Normally transformers are relatively large and expensive components in a circuit or system. But there are several outstanding advantages using transformers in circuit design: direct current (dc) isolation between primary and secondary winding, balanced-unbalanced (balun) function, impedance transformation and no power consumption.

The requirements of nowadays telecommunication systems needs a high degree of monolithic integration. Today it is possible to integrate lumped planar transformers in silicon-based integrated circuit (IC) technologies which have excellent performance characteristics in the 1-20 GHz frequency range. The outer dimensions are in the range of about 500 μm down to 60 μm diameter depending on the frequency of operation and the IC technology.

Monolithic integrated lumped planar transformers are introduced by e.g. [1]. A review of the electrical performance of passive planar transformers in IC technology was presented

by [2]. Amplifiers and mixers using monolithic transformers are presented in [3, 4]. A monolithic 2 GHz Meissner-type voltage controlled oscillator is realized in e.g. [5].

The transformer coupled push-pull type rf power amplifier was invented in the early days of tubes which has survived into the semiconductor era with its benefits. There appears a 4:1 load-line impedance benefit for a push-pull combining scheme in an equal-power comparison to simple parallel device connection [6]. In general, impedance mismatch losses at the output of the power amplifier due to the decrease of the impedance required at low supply voltages limits the output power and the power-added efficiency (PAE). Due to the balanced amplifier design each output transistor contributes only half the total output power. The emitter bondwire inductance is not so critical because of the differential output stage. However, this approach requires a balun at the output of the power amplifier. For the first time, monolithic integration in Si-based technologies becomes successful [7, 8, 9]. But up to now there was no way to get an accurate prediction and model of the electrical characteristic of on-chip transformers.

Section 2 presents the modelling and model verification of integrated lumped planar transformers in Si-based technologies which have excellent performance characteristics. A lumped low-order model, which consists of 24 elements gives an accurate prediction of the electrical behaviour and ensures a fast transient analysis, because of the low complexity. The method of parameter extraction for the equivalent circuit is based on a tool developed by the authors which uses a new expression for the substrate loss and two finite element method (FEM) cores called *FastHenry* [10] and *FastCap* [11].

In Section 3 a monolithic rf power amplifier for 1.8–2 GHz is presented which has been realized in a 50 GHz-f_T Si bipolar technology. The chip is operating down to supply voltages as low as 1.2 V. The balanced 2-stage power amplifier uses two on-chip transformers as input-balun and for interstage matching, with a high coupling coefficient of $k = 0.84$. At 1.2 V, 2.5 V, and 3 V supply voltage an output power of 0.22 W, 1 W and 1.4 W is achieved, at a PAE of 47 %, 55 % and 55 %, respectively, at 1.9 GHz. The small-signal gain is 28 dB. Section 4 shows a power amplifier design optimized for high output power at 900 MHz and low supply voltages. The chip is operating from 2.8 V to 4.5 V. At 2.8 V the output power is 3.2 W with a PAE of 54 %. The maximum output power of 7.7 W with an efficiency of 57 % is achieved at 4.5 V supply voltage. The small-signal gain is 38 dB. In Section 5 a lumped LC balun as output matching network is reviewed and extended to a dual-band balun.

2. MONOLITHIC INTEGRATED TRANSFORMER DESIGN

Monolithic transformers have been presented in various geometric designs and many different kinds have been realized. A special planar winding scheme for monolithic transformers which results in a very high coupling coefficient k is discussed in this section.

To realize other values than N=1:1 of the turn ratio, different numbers of primary and secondary turns are used. This implements that some adjacent conductors belong to the same winding which results in a lower k-factor. A solution for this problem is to use an interlaced winding-scheme. One winding (e.g. the secondary) is sectioned into a number of individual turns connected in parallel rather than one continuous winding. Each segment of the secondary windings is interlaced with a primary turn. The line width of each segment is designed to carry the same current to obtain a homogeneous magnetic field distribution. The monolithic transformer shown in Fig. 1 consists of six primary turns P1-P6 and two secondary turns S1-S2. The turn ratio is N=6:2. The center taps PCT and SCT are available.

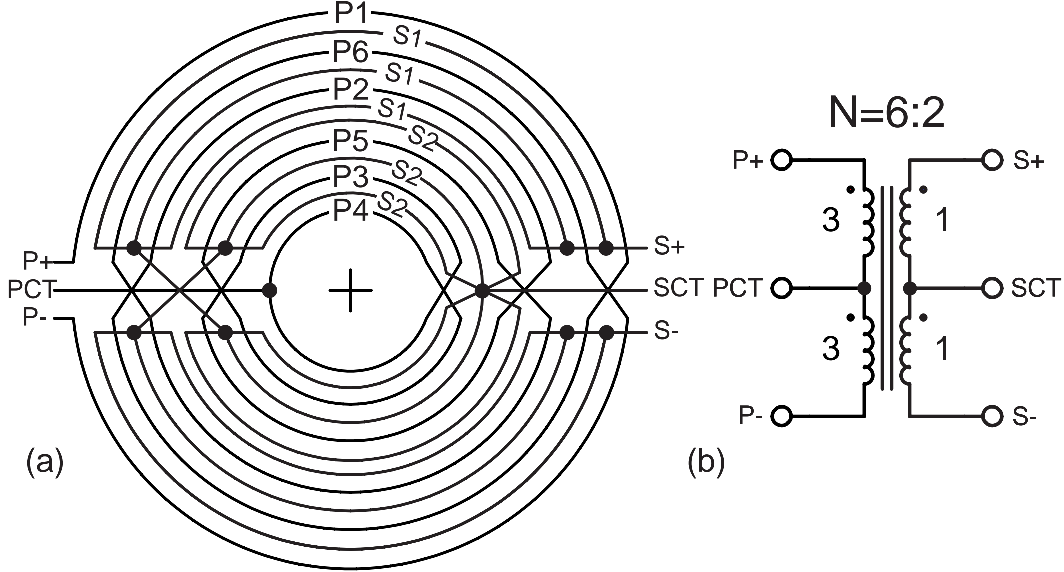

Figure 1: Planar high coupling performance transformer: (a) Winding scheme (b) Schematic symbol.

Fig. 2 shows a three-dimensional topview of the transformer. The primary ports, P+, PCT and P-, are located on the left side. The secondary ports, S+, SCT and S-, are located on the right side. The transformer design is nearly symmetric about a line. The outer diameter is $2r_O = 205\,\mu$m and the inner diameter is $2r_I = 50\,\mu$m. The lateral spacing between the turns is about $1.5\,\mu$m and has different values for each metal layer because of different design rules (Fig. 4). The conductor width on the primary side is about $W = 6\,\mu$m. The conductor width on the secondary side about $W = 4\,\mu$m and different for each winding to get the same series resistance of each segment of the secondary turns.

Fig. 3 shows a cross-section of this transformer. The primary winding consists of metal 3 and metal 2 connected in parallel and is separated to the substrate by H_{ox}=3.1 μm. The secondary winding consists of metal 1-3 connected in parallel to decrease ohmic loss. The substrate distance is H_{ox}=1.6 μm. The secondary winding consists of metal 1-3 connected in parallel to decrease ohmic loss. A cross section of the substrate and metal layer stack is shown in Fig. 4.

2.1. Lumped Low-Order Equivalent Model

An electrical model of a transformer can be recognized from the physical layout. The circuit devices in Fig. 3 are the basic elements of the equivalent circuit shown in Fig. 5 and can be identified as: multiple coupled inductors L_1 to L_4, ohmic loss in the conductor material R_{S1} to R_{S4}, parasitic capacitive coupling between the windings C_{K1} to C_{K4} and into the substrate C_{OX1} to C_{OX6} and finally substrate losses R_{Sub1} to R_{Sub6}. With this basic elements a lumped low-order equivalent model was constructed.

Limits of the Transformer Model

In general the transformer model is valid down to dc. The upper frequency limit of the model depends on the transformer geometry. For valid simulation results the maximum outer dimensions of the transformer must be $\ll \lambda$, the guided wavelength. In most cases

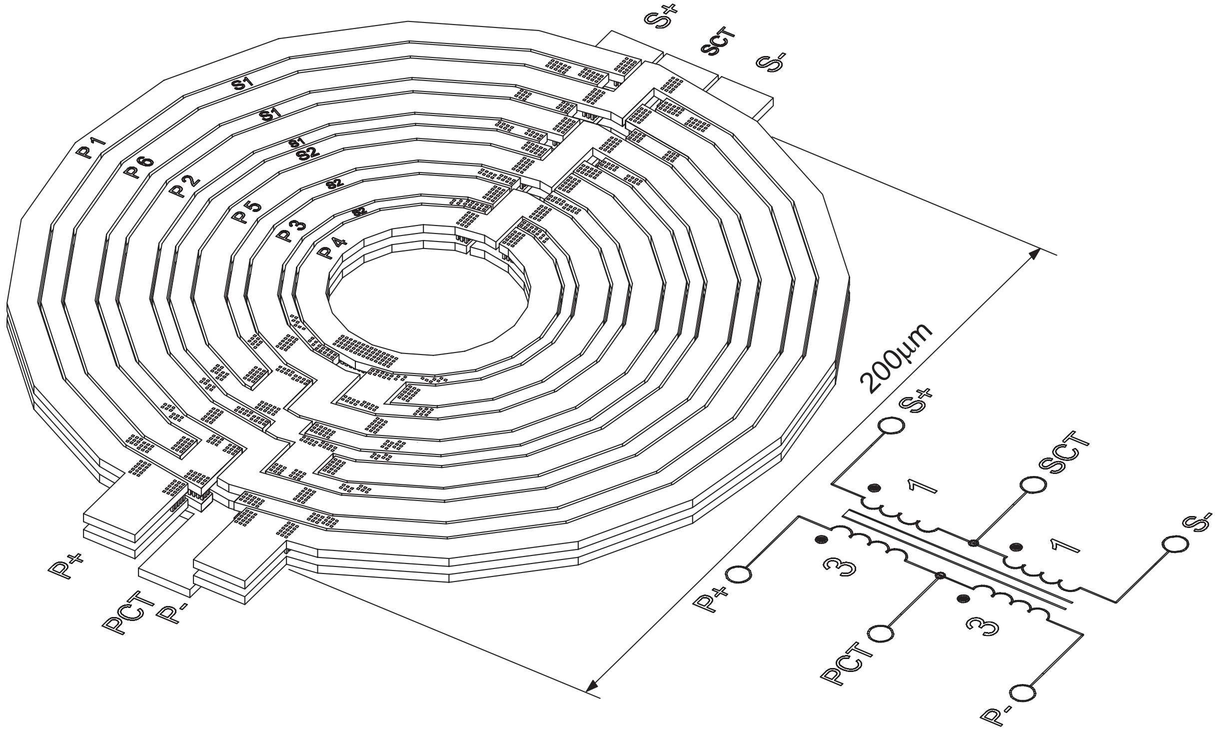

Figure 2: 3-D-view of the planar high coupling performance transformer

the upper limit of the proposed model is about 3/2 times the self resonant frequency of the transformer.

2.2. Parameter Extraction

The lumped low-order equivalent model (Fig. 5) describes the electrical behaviour of the monolithic integrated lumped transformer. This section gives the background details about extraction of all elements used in the equivalent-circuit.

Inductance and Series Resistance

Transformers composed of straight conductors can be treated with the summation of self- and mutual-inductances of all individual conductor elements. The whole transformer geometry built up of straight conductors is the input to the FEM-core *FastHenry* [10]. The exact modeling of the planar construction is an important task for an accurate inductance extraction. The exact modeling of the layer construction is less important for the inductance calculation. Each inductance L_1-L_4 is coupled mutually with every other inductance, denoted by the coupling coefficients $k_{ik} = M_{ik}/\sqrt{L_i L_k}$ where M_{ik} is the extracted mutual inductance. Ohmic losses in the conductor material due to skin effect, current crowding and finite conductivity are modeled by the series resistances R_{S1}-R_{S4} at the frequency of operation of the transformer.

Capacity Extraction

Capacities are difficult to determine accurately and capacitive effects are best investigated in mesh point analysis. The exact modeling of the layer construction is important to get accurate results. In order to reach short processing times only a small part of the transformer's cross section is the input to the FEM-core *FastCap* [11]. The static specific

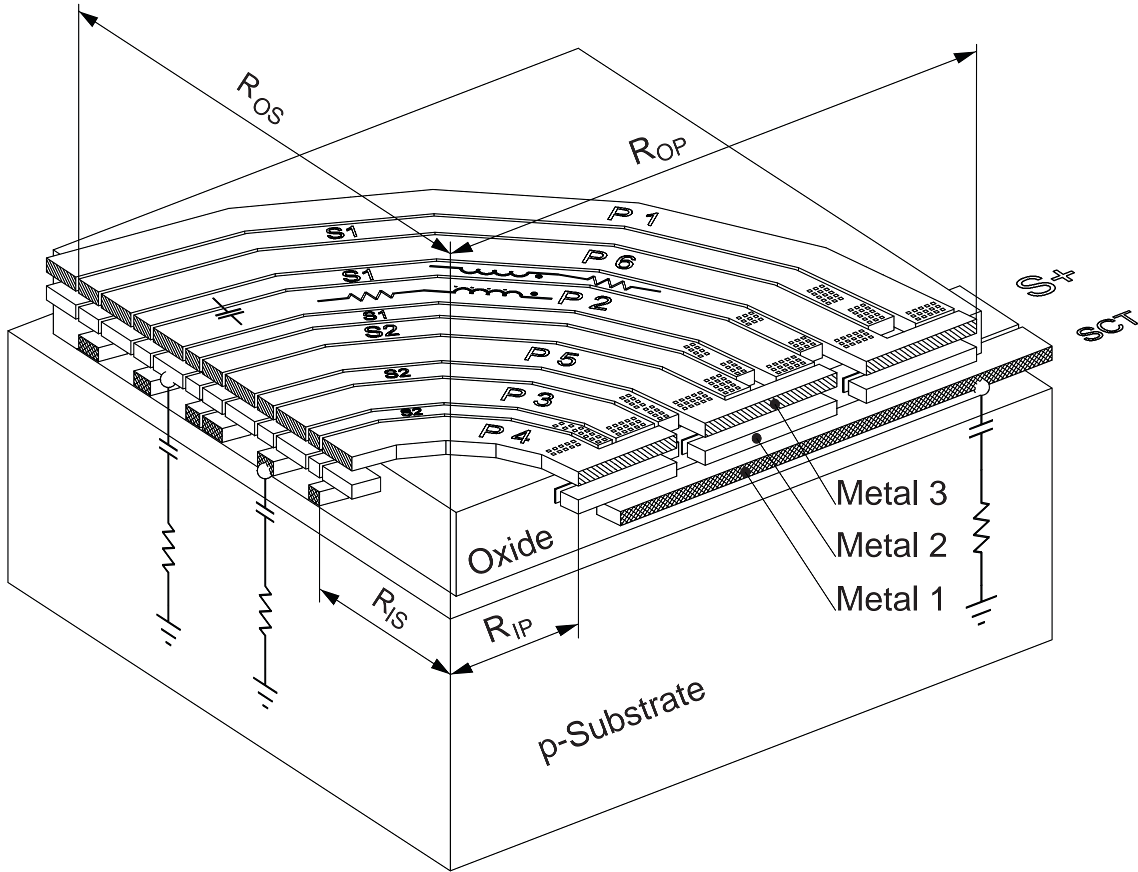

Figure 3: 3-D section of the high coupling performance transformer with basic model elements.

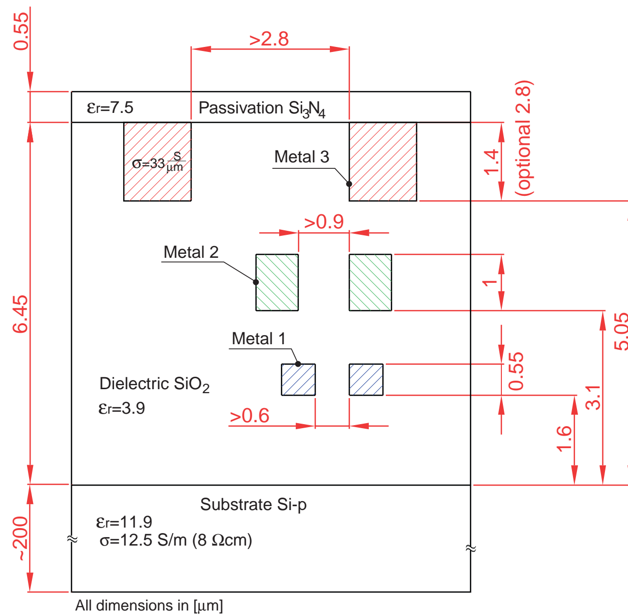

Figure 4: Schematic cross section of the substrate including the metal layer stack.

capacities from primary to secondary C'_{PS} primary C'_P and secondary C'_S to substrate are extracted. The capacities of the transformer are $C_P = l_{MP}\,C'_P$, $C_S = l_{MS}\,C'_S$ and

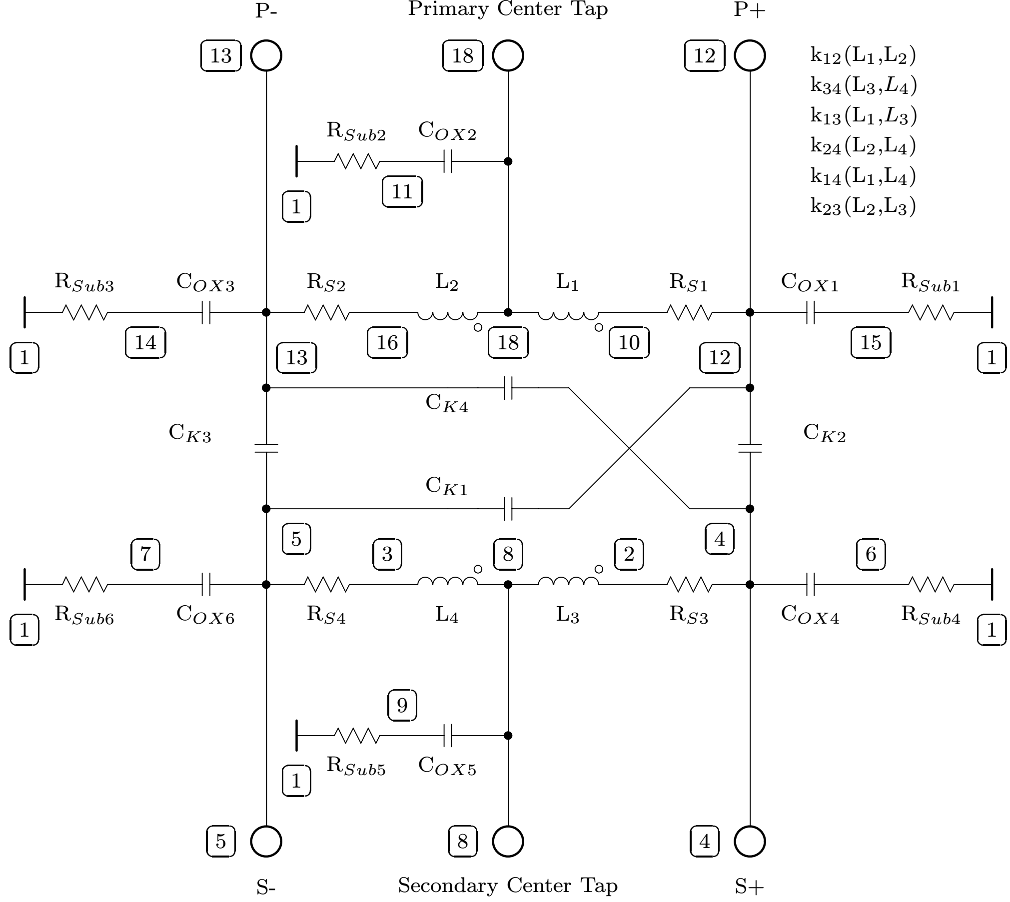

Figure 5: The lumped equivalent circuit of the transformer (node 1 = substrate)

$C_{PS} = l_M\, C'_{PS}$ where l_{MP}, l_{MS} and l_M are the mean perimeters of the included transformer turns. In the case of a circular transformer as shown in Fig. 3 they are calculated as

$$l_{MP} = \pi(R_{OP} + R_{IP}),\ \ l_{MS} = \pi(R_{OS} + R_{IS}) \tag{1}$$

$$l_M = \pi\left[\max(R_{OP}, R_{OS}) + \min(R_{IP}, R_{IS})\right] \tag{2}$$

C_{OX1} to C_{OX6} of Fig. 5 are determined as $C_{OX1} = C_{OX3} = C_P/4$, $C_{OX2} = C_P/2$ and $C_{OX4} = C_{OX6} = C_S/4$, $C_{OX5} = C_S/2$. The sum of the capacities C_{OX} for each winding is the static capacity C_P and C_S to the substrate.

The parasitic capacitive coupling between primary and secondary winding are determined as C_{K1} to C_{K4}=$C_{PS}/4$.

Substrate Loss

Fig. 6 shows a conductor (i.e. a turn of a transformer) suspended in a dielectric. Capacitive coupling causes a current flow down to the ground plane shown in Fig. 6 as lines of constant current density.

From Fig. 6 is clear that the current-feed-in area at the substrate edge has a greater width than the physical width W. We define a effective feed-in width W_{eff} depending on

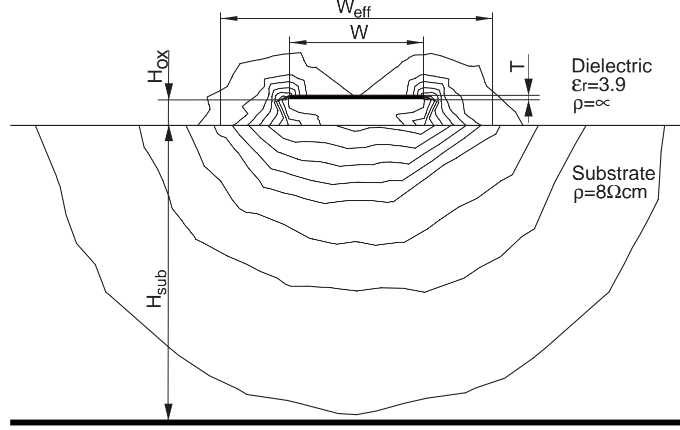

Figure 6: Current density around a conductor suspended in a dielectric. H_{OX}=4 μm, H_{Sub}=200 μm, W=20 μm, T=0.1 μm;

the distance H_{OX} and conductor height T.

$$W_{eff} = W + 6\,H_{OX} + T \tag{3}$$

The specific resistance R'_{Sub} in [Ωmm] from a single conductor to ground as shown in Fig. 6 can be written as

$$R'_{Sub} = \frac{\rho}{2\pi} \ln\left[2\coth\left(\frac{\pi}{8}\frac{W_{eff}}{H_{Sub}}\right)\right] \tag{4}$$

The error of (4) is always smaller than 3 % in the range of $W_{eff}/H_{Sub} < 1$.

R_{Sub} of a complete transformer winding is based on (3) and (4) where W is the complete width of the primary $W_P = R_{OP} - R_{IP}$ or secondary winding $W_S = R_{OS} - R_{IS}$ as shown in Fig. 3. R_{SubP} for the primary winding can be written as ([12])

$$R_{SubP} = \frac{\rho}{2\pi l_{MP}} \ln\left[2\coth\left(\frac{\pi}{8}\frac{W_P + 6\,H_{OX} + T}{H_{Sub}}\right)\right] \tag{5}$$

and similar R_{SubS} for the secondary winding, respectively. R_{Sub1} to R_{Sub6} of Fig. 5 are determined as $R_{Sub1} = R_{Sub3} = 4R_{SubP}$, $R_{Sub2} = 2R_{SubP}$ and $R_{Sub4} = R_{Sub6} = 4R_{SubS}$, $R_{Sub5} = 2R_{SubS}$. More detailed information on modelling and parameter extraction of monolithic transformers can be found in [12].

2.3. Transformer Model Verification

The transformer is placed on silicon using two test structures including deembedding structures to measure the scattering parameters. One test structure is used to evaluate the primary-to-secondary transmission coefficient, where one input terminal of the primary and secondary winding is grounded, respectively. The second test structure is used to characterize the primary winding and secondary winding separately, where the opposite winding is left open, respectively. The center taps are always left open. In general, a 4-port measurement setup would give a little bit more accuracy, but would require much more measurement efforts.

The equivalent circuit of the high coupling performance transformer is shown in Fig. 7. All parameter values are extracted by using the method described in Section 2.2. Node 1

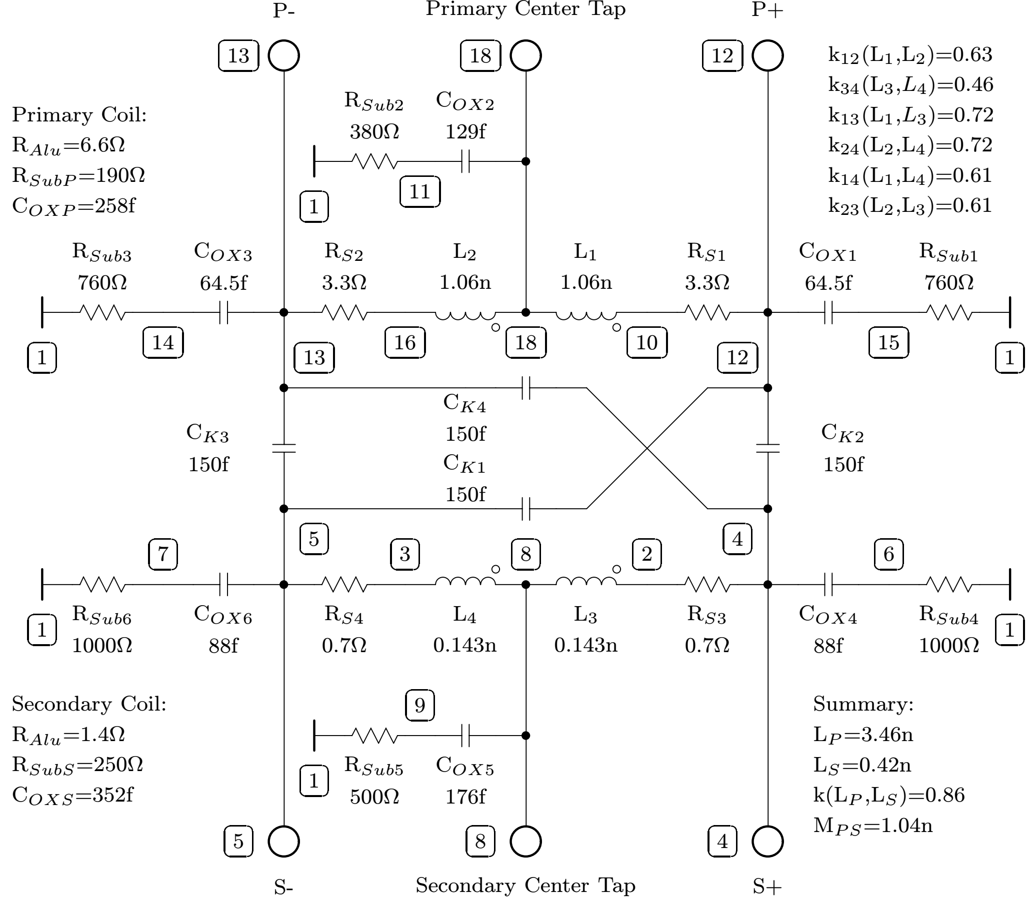

Figure 7: Equivalent circuit of the high coupling performance transformer.

is connected to the substrate. The values of the primary and secondary self inductance are

$$L_P = L_1 + L_2 + 2\,k_{12}\sqrt{L_1\,L_2} = 3.46\,\text{nH} \tag{6}$$

$$L_S = L_3 + L_4 + 2\,k_{34}\sqrt{L_3\,L_4} = 0.42\,\text{nH} \tag{7}$$

The strength of magnetic coupling between primary and secondary side denoted by the k-factor is

$$k_{PS} = \frac{k_{13}\sqrt{L_1\,L_3} + k_{14}\sqrt{L_1\,L_4} + k_{23}\sqrt{L_2\,L_3} + k_{24}\sqrt{L_2\,L_4}}{\sqrt{L_P\,L_S}} = 0.86 \tag{8}$$

The series resistance of the conductors on the primary side is $R_{Alu} = 6.6\,\Omega$ and on the secondary side $R_{Alu} = 1.4\,\Omega$. Tue due the greater distance to the substrate the parasitic capacity of the primary winding $C_{OXP} = 258\,\text{fF}$ is less than the capacity of the secondary winding $C_{OXS} = 352\,\text{fF}$. The substrate resistances R_{Sub} of both windings are in the same range of about $200\,\Omega$.

Fig. 8 shows the measured and simulated reflection S11 and S22 of the high coupling performance transformer. Measurement and model shows excellent agreement up

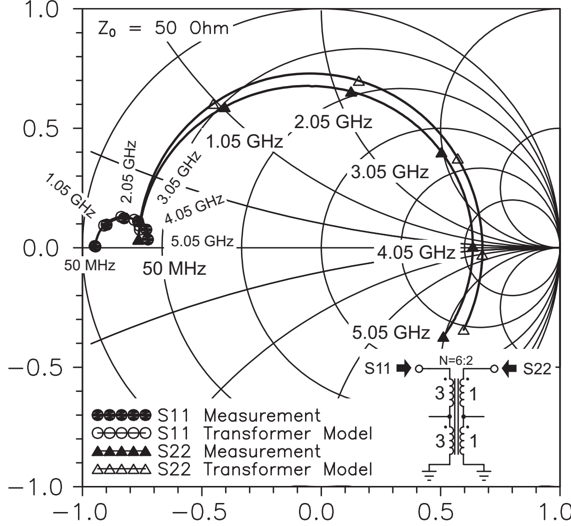

Figure 8: Measured and simulated scattering parameters S11 and S22 of the transformer.

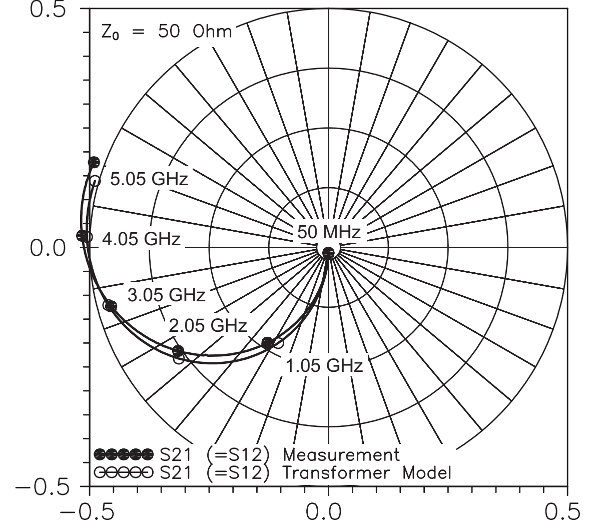

Figure 9: Measured and simulated transmission coefficient S21 of the transformer.

to 5 GHz. Fig. 9 shows S21. The insertion loss is about 9 dB at 1.9 GHz. The difference between simulation and model is negligible. The S-parameters describe the electrical behavior of a monolithic transformer completely. But, not only the scattering parameters must be observed. Also the Z-parameters, Y-parameters, k-factor and Q-factor derived directly from the S-parameters give a fundamental insight to the transformer's characteristic.

Fig. 10 shows primary inductance L_p and secondary L_s as a function of frequency. The self inductances are analyzed using

$$L_P = L_1 + L_2 + 2\,k_{12}\sqrt{L_1\,L_2} = \frac{\mathrm{Im}\,(Z_{11})}{\omega} \tag{9}$$

$$L_S = L_3 + L_4 + 2\,k_{34}\sqrt{L_3\,L_4} = \frac{\mathrm{Im}\,(Z_{22})}{\omega} \tag{10}$$

The simulated and measured self resonance is at 4 GHz.

Analyzing the coupling coefficient as a function of frequency the relation

$$M = k_{13}\sqrt{L_1 L_3} + k_{14}\sqrt{L_1 L_4} + k_{23}\sqrt{L_2 L_3} + k_{24}\sqrt{L_2 L_4} = \sqrt{(Y_{11}^{-1} - Z_{11})\frac{Z_{22}}{\omega^2}} \tag{11}$$

is useful. Then the coupling coefficient can be written as

$$k(L_P, L_S) = \frac{M}{\sqrt{L_P L_S}} = \sqrt{\frac{(Y_{11}^{-1} - Z_{11})Z_{22}}{Im(Z_{11})Im(Z_{22})}} \tag{12}$$

Fig. 11 shows the coupling coefficient versus frequency. A k-factor of 0.9 at 1.9 GHz is a very high value for monolithic lumped planar transformers.

Especially Y_{11}^{-1}, which represents the input impedance of the secondary short-circuit transformer, becomes significant importance because of the low input impedance of the

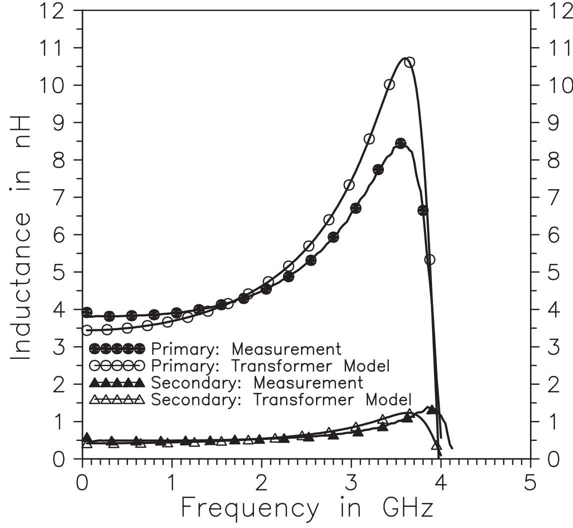

Figure 10: Self inductance of the primary and secondary winding of the transformer.

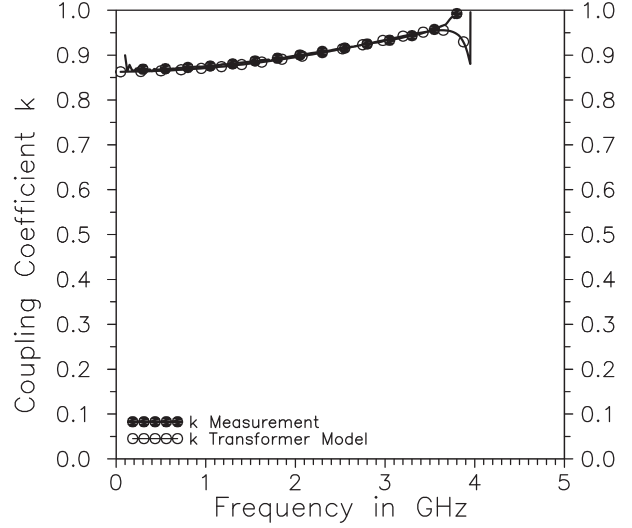

Figure 11: Coupling coefficient k versus frequency of the transformer.

driver stage and output stage of the power amplifier. Fig. 12 shows the real part of the measured and simulated real part of Y_{11}^{-1} and Y_{22}^{-1}. Fig. 13 shows the imaginary part. Simulation and measurement agrees very well up to 3 GHz. The quality factor of the

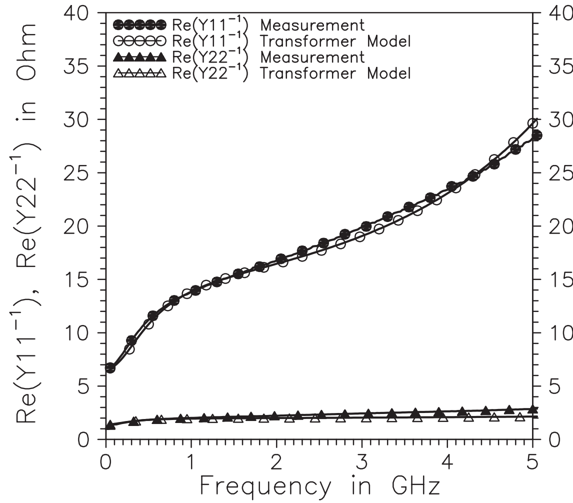

Figure 12: Real part of the primary and secondary input impedance with short circuit at the opposite side, respectively.

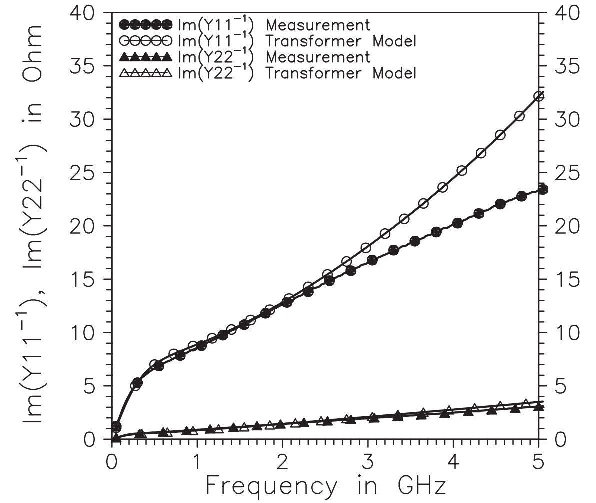

Figure 13: Imaginary part of the primary and secondary input impedance with short circuit at the opposite side, respectively.

transformer with the secondary winding open circuit Q_{open} and short circuit Q_{short} can be analyzed using the following expressions

$$Q_{open} = \frac{\mathrm{Im}\left(Z_{11}\right)}{\mathrm{Re}\left(Z_{11}\right)} \tag{13}$$

$$Q_{short} = \frac{\mathrm{Im}\left(Y_{11}^{-1}\right)}{\mathrm{Re}\left(Y_{11}^{-1}\right)} \tag{14}$$

$Q_{open} \approx 3$ and $Q_{short} \approx 0.8$ of this transformer at 2 GHz. In most cases the upper limit of the model is about 2/3 times the self resonant frequency of the transformer.

2.4. Transformer Tuning

In many applications, i.g. input matching and interstage matching of a power amplifier, a high current transfer ratio of the on-chip transformer is desired. In contrast to an ideal transformer the current transfer ratio of a lossy transformer is not equal to the value of the turn ratio. Fig. 14 shows a secondary short-circuit transformer. It consists of a primary winding L_P and a secondary winding L_S. L_P and L_S are mutually coupled, denoted by the k-factor. In most cases the input impedance of the driver stage and the output stage is very low. Therefore, the secondary winding of the transformer in Fig. 14 is short-circuit, but without loss of generality. The ohmic loss of the primary winding L_P, ohmic loss the secondary winding L_S and the input impedance of the transistors (assumed real valued) are considered by the admittance G. The transformer is connected as a parallel resonant device using the capacitor C.

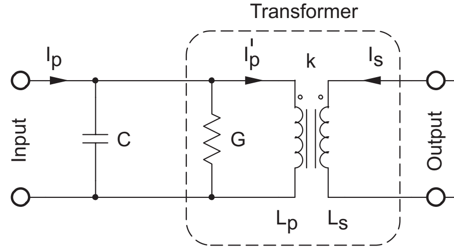

Figure 14: Tuned ideal transformer equivalent circuit.

Then the resonant frequency ω_{res} of the tuned transformer can be derived as

$$\omega_{res} = \frac{1}{\sqrt{(1-k^2)\cdot C \cdot L_P}} \tag{15}$$

The quality factor Q of the resonant circuit is

$$Q = \frac{\omega_{res} \cdot C}{G} = \frac{1}{G} \cdot \sqrt{\frac{C}{(1-k^2)\cdot L_P}} \tag{16}$$

The inner current transfer ratio of the ideal transformer is

$$\frac{I_S}{I'_P} = -k \cdot \sqrt{\frac{L_P}{L_S}} \tag{17}$$

Now the total current transfer ratio I_S/I_P of the parallel resonant transformer can be expressed by

$$\left|\frac{I_S}{I_P}\right| = k \cdot Q \cdot \sqrt{\frac{L_P}{L_S}} \tag{18}$$

This relation shows, that in contrast to the untuned transformer, the total current transfer ratio can be increased by a quality factor of $Q > 1$.

3. A 2 V, 1 W SI-BIPOLAR POWER AMPLIFIER AT 1.9 GHZ

This section presents a circuit design using the transformer described in Section 2. Fig. 15 shows the schematic diagram of the power amplifier for 1.9 GHz. The circuit consists of a transformer X1 as input-balun, a driver stage T1 and T2, a transformer X2 as interstage matching network and a power output stage T3 and T4. The transformers X1 and X2 are of the same kind (Sect. 2). X1 is connected as a parallel resonant device using the MOS capacitor $C_{IN} = 1.4\,\mathrm{pF}$ (Sect. 2.4). The transformer acts as balun as well as input matching network. The interstage power transformer X2 is connected as a parallel resonant device using $C_{IS} = 0.75\,\mathrm{pF}$. C_{IN} and C_{IS} are realized using two MOS capacitors connected in antiseries, respectively.

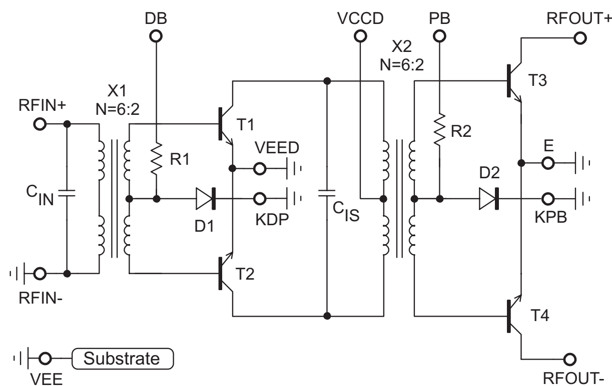

Figure 15: Power amplifier schematic diagram.

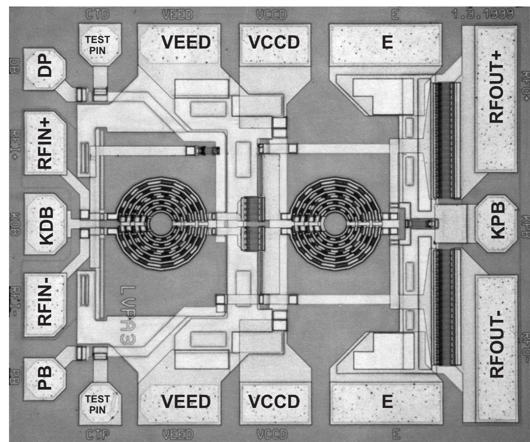

Figure 16: Die photograph (chip size: $1.17 \times 0.97\,\mathrm{mm}^2$).

The effective emitter area of the driver stage is two times $96\,\mu\mathrm{m}^2$. The emitter area of the output stage is two times $480\,\mu\mathrm{m}^2$. The bias operating point of the driver stage and the output stage is adjusted using the current mirrors R1, D1 and R2, D2 respectively, connected via the center taps of the transformers.

Fig. 16 shows the die photograph of the amplifier. The chip size is $1.17 \times 0.97\,\mathrm{mm}^2$. The power amplifier has been fabricated in an advanced production-near silicon bipolar technology [13]. The transistors have a double-polysilicon selfaligned emitter-base-configuration similar to a lot of current production technologies of various companies. As only standard process tools are used the technology is highly manufacturable at low costs. The minimum lithographic feature size is $0.5\,\mu\mathrm{m}$. The doping of the speed-limiting base profile is done by low-energy ion implantation and subsequent diffusion using rapid thermal processing. This enables a final base width of only 50 nm at an intrinsic base sheet resistance of $14\,\mathrm{k}\Omega/\square$. The devices have transit frequencies and maximum oscillation frequencies (extracted from the maximum available gain) of 50 GHz and provide an ECL gate delay of 16 ps. The collector-base breakdown voltage is $BV_{CB0} = 11\,\mathrm{V}$ and the collector-emitter breakdown voltage is $BV_{CE0} = 2.7\,\mathrm{V}$. A supply voltage of more than BV_{CE0} is possible, if low impedance driving conditions are present [14].

The power amplifier was tested at $f_0 = 1.8\,\mathrm{GHz}$ to 2 GHz using chip-on-board packaging on a two-sided Rogers RO4003 test board. Conductive epoxy is used for the die attach. The input of the amplifier chip is connected via a $50\,\Omega$ micro-strip line to the input signal. The supply-voltage line of the output stage consists of two $50\,\Omega$ $\lambda/4$-length

lines, translating a low impedance at $2f_0$ to the output transistors. The optimum load impedance at f_0 is translated by a balanced $25\,\Omega$ odd-mode micro-strip line. Two lumped capacitors are used to set the real part and the imaginary part of the optimum load impedance at f_0. A compensated $\lambda/4$-length semi-rigid line acts as balun.

Fig. 17 shows the measured output power and efficiency as a function of rf input power at 1.9 GHz, and as a function of power supply voltage. The matching network is

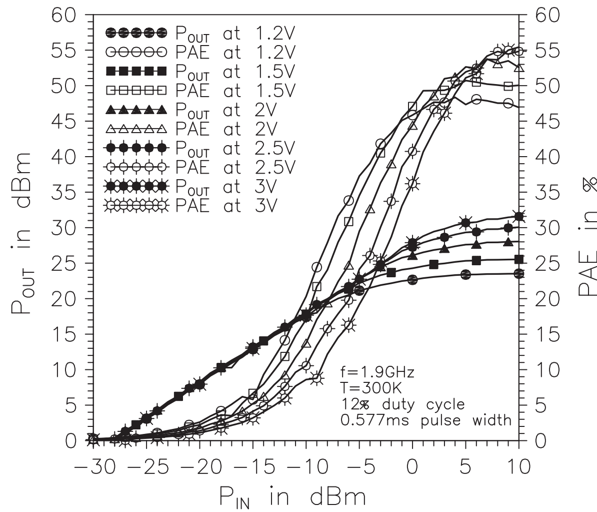

Figure 17: Measured output power and PAE versus input power and supply voltage.

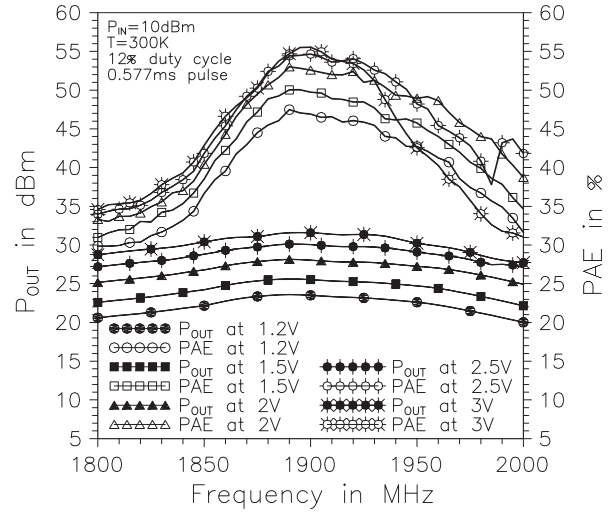

Figure 18: Measured output power and PAE versus frequency and supply voltage.

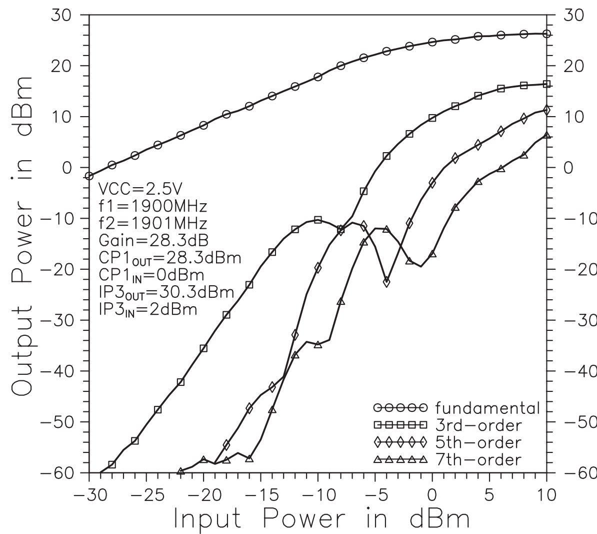

Figure 19: Measured two-tone intermodulation performance.

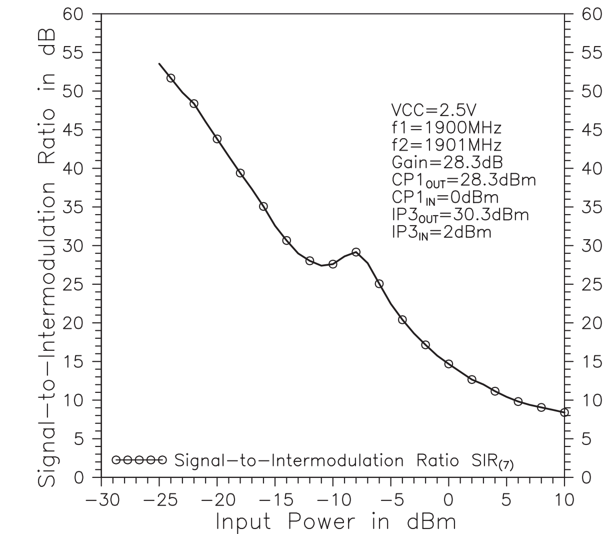

Figure 20: Measured 7th-order signal-to-intermodulation ratio.

unchanged for all supply voltages and the complete frequency range. The power amplifier is operating in a pulsed mode with a duty cycle of 12.5 %. The pulse width is 0.577 ms. The bias operating current, without rf excitation, is two times 20 mA at the driver stage and two times 75 mA at the output stage. The bias operating currents are adjusted to these values at each level of supply voltage. When operating from a 1.2 V supply, the amplifier

has a maximum output power of 0.22 W (23.4 dBm), and a power-added efficiency of 47 % at 1.9 GHz. At 3 V supply voltage, the output power is 1.4 W (31.5 dBm) at a power-added efficiency of 55 %. Fig. 18 shows the output power and PAE versus the frequency from 1.8 GHz to 2 GHz.

Fig. 19 shows the two-tone intermodulation performance of the power amplifier at 1.9 GHz and 2.5 V supply voltage. The 3rd-order output intercept point $IP3_{OUT}$ is +30 dBm. The 7th-order signal-to-intermodulation ratio SIR_7 extracted from the measurements in Fig. 19, is shown in Fig. 20. The ratio is 8.5 dB in the fully saturated region. Table 1 summarizes the measurement results of the power amplifier.

Operating Frequency	1.8 GHz – 2 GHz					
Supply Voltage	1.2 V – 3 V					
Small-Signal Gain (1.9 GHz)	28 dB					
Chip Size	1.17 mm × 0.97 mm					
Technology	Si bipolar 0.5 μm, f_T=50 GHz, f_{max}=51 GHz					
Supply Voltage	1.2	1.5	2	2.5	3	V
Maximum Output Power at 1.9 GHz and Pin=10 dBm	0.22 (23.4)	0.35 (25.4)	0.63 (28)	1 (30)	1.4 (31.5)	W (dBm)
Power-Added Efficiency at 1.9 GHz and Pin=10 dBm	47	50	52	55	55	%
Output-Stage Collector Efficiency at 1.9 GHz and Pin=10 dBm	61	64	65	67	67	%

Table 1: Performance summary (T=300 K, 12.5 % duty cycle, 0.577 ms pulse width).

If a simple lumped LC-balun (Fig. 29) is used as matching network, then the maximum PAE is about 40 % and the maximum output power is decreased by about 1 dB to 2 dB at each level of supply voltage, respectively.

4. A 2.8 V, 3.2 W SI-BIPOLAR POWER AMPLIFIER AT 900 MHZ

In this section a circuit design for 900 MHz, optimized for high output power at low supply voltages around 3 V is presented using the transformer described in Section 2, except that the shape of the transformer is enlarged by a factor of two. The outer diameter of the transformer is 410 μm now. Fig. 21 shows the model of the enlarged transformer. The series resistance of the conductors on the primary side is $R_{Alu} = 7\,\Omega$ and on the secondary side $R_{Alu} = 1.7\,\Omega$. The primary inductance is 7 nH, the secondary inductance is 1 nH. The coupling factor is $k = 0.84$. The self resonant frequency is 1.8 GHz. The frequency of operation of this transformer should be less than 1.2 GHz for good circuit performance.

Fig. 22 shows the simplified schematic diagram of the balanced 2-stage power amplifier. The rf-part of the power amplifier consists of an on-chip transformer X1 as input-balun, a driver stage T1, T2, two transformers X2, X3 as interstage matching network and a power output stage T3, T4. The effective emitter area of the output stage is two times 2520 μm^2. The input-transformer is connected as a parallel resonant device using two MOS capacitor connected in antiseries. The transformer acts as balun as well as input matching network.

The interstage matching network of the power amplifier consists of two transformers

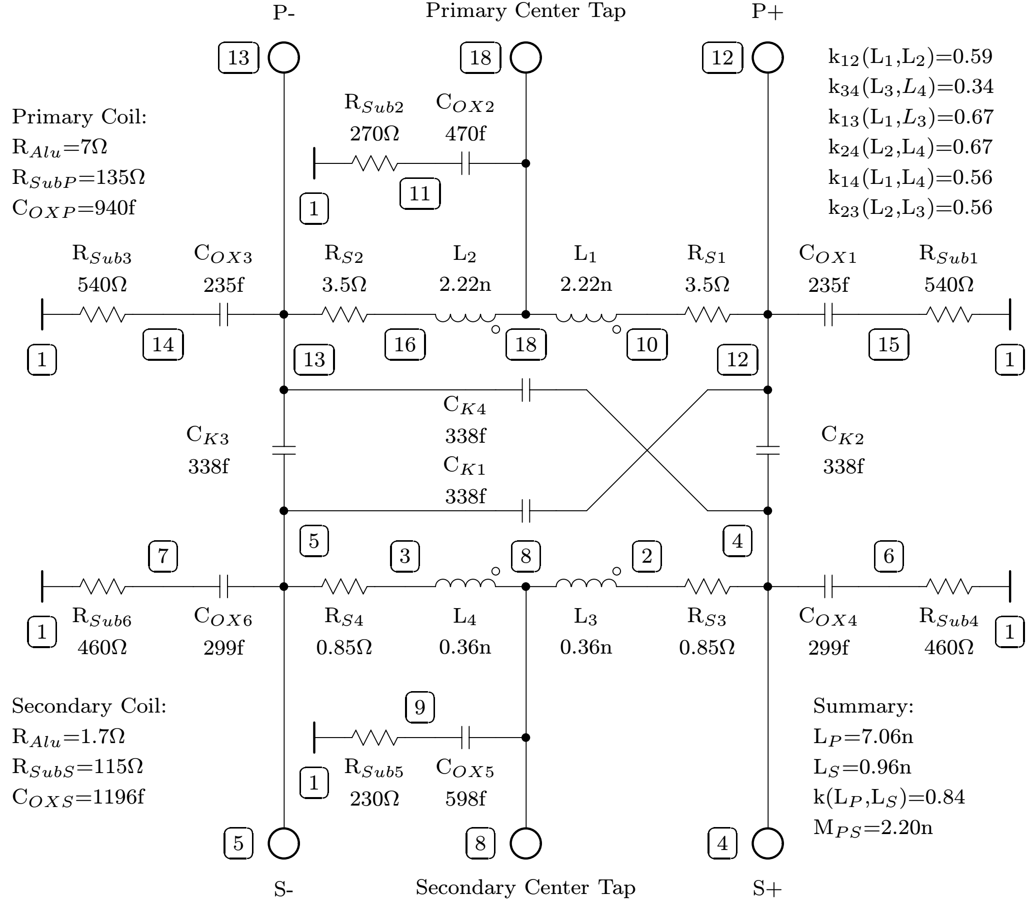

Figure 21: Equivalent model of the 900 MHz transformer (outer diameter 410 μm).

X2 and X3 connected in parallel, to get a high current transfer ratio at a low signal voltage swing.

To diminish break-down effects at high supply voltages a closed loop bias operating point circuit is implemented. The maximum usable output voltage of the driver and the power stage depends on the driving conditions [14]. Thus, the source impedance of the bias driver should be as low as possible. The bias current of the driver stage is set by an operational amplifier U1 and T7, T8 via the secondary center tap of X1. T5 acts as current sensing device. The collector current of T5 is compared with the bias operating point reference current I_{REF}. This closed loop ensures a low impedance driving condition and a constant collector bias current over a wide range of supply voltage, for the driver stage T1, T2. R1 matches the output characteristic (breakdown) of the sensing device T5 to the driver stage transistors T1, T2. The bias circuit of the power stage T3, T4 is of the same kind.

Fig. 23 shows a die photograph of the power amplifier. The chip measures $2.1\times2.0\,\mathrm{mm}^2$. The chip is fabricated in a standard 25 GHz-f_T, 0.8 μm, 3-layer-interconnect silicon bipolar production technology of Infineon B6HF [15]. The collector-base breakdown voltage is $BV_{CB0} = 18\,V$ and the collector-emitter breakdown voltage is $BV_{CE0} = 3.9\,V$.

For measurements the chip is bonded on a FR4 test board (see Fig. 26, Fig. 24, Fig. 25).

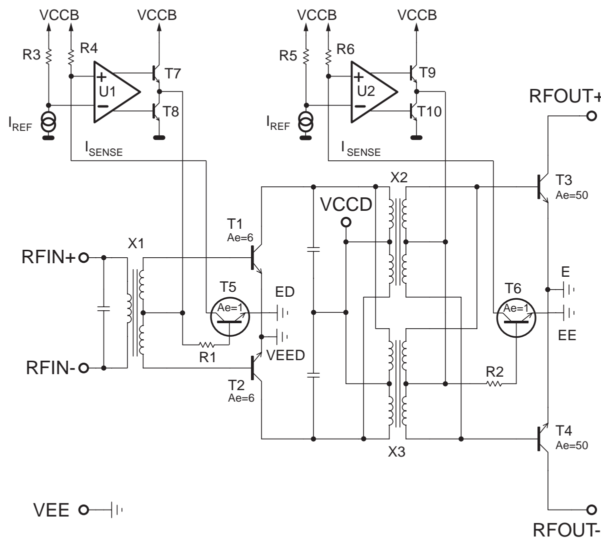

Figure 22: Schematic diagram of the 900 MHz power amplifier.

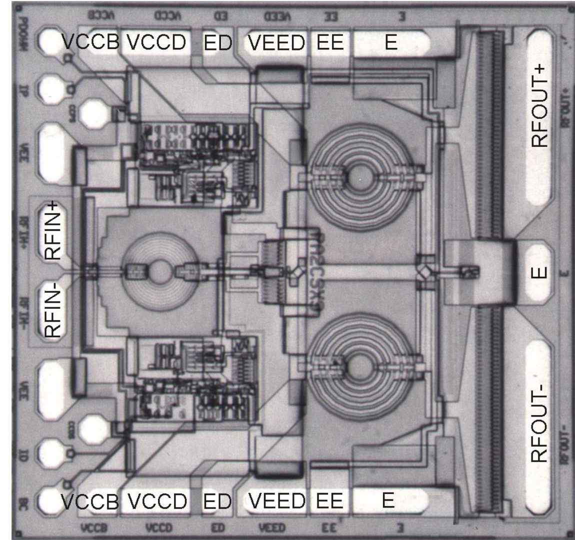

Figure 23: Chip photograph, chip size: 2.1 $\times$ 2.0 mm^2.

The input of the amplifier chip is connected via a 50 Ω micro-strip line to the input signal of $f_0 = 0.8 - 1$ GHz. The supply-voltage line of the output stage consists of two 50 Ω $\lambda/4$-length lines translating a low impedance at $2f_0$ to the output transistors. The optimum load impedance at f_0 is translated by a balanced 25 Ω $\lambda/8$-length micro-strip line. The real and imaginary part of the load impedance is determined nearly orthogonal by two capacitors. A compensated $\lambda/4$-length semi-rigid line acts as balun. This balun-line can be replaced by a lumped LC-balun with slight loss of performance. A more detailed description and evaluation of performance of this matching network compared to a lumped LC balun is presented in [7].

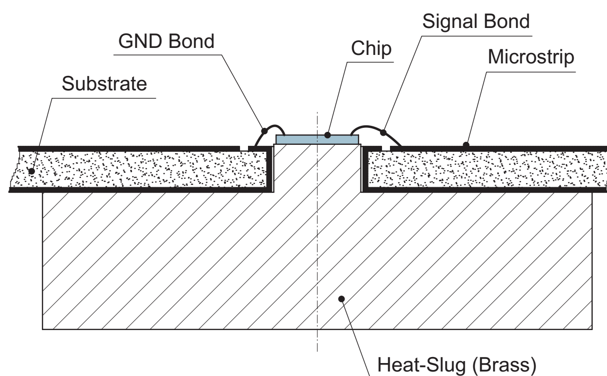

Figure 24: Cross section of the chip mounted on a brass heat-slug.

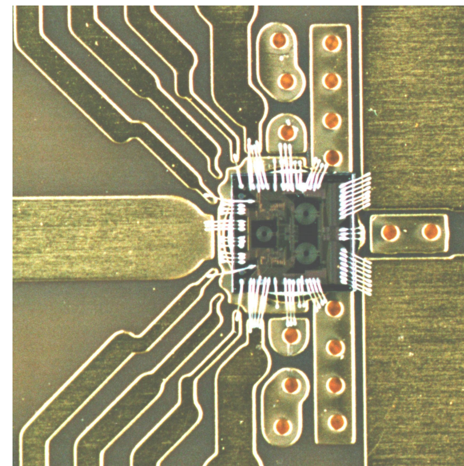

Figure 25: Detail view: power amplifier chip bonded on the FR4 testboard with heat-slug.

Fig. 27 shows the output power and PAE versus input power as a function of supply voltage at 900 MHz. The matching network is unchanged for all supply voltages. At 2.8 V supply voltage an output power of 3.2 W with 54 % PAE is achieved. The small-signal

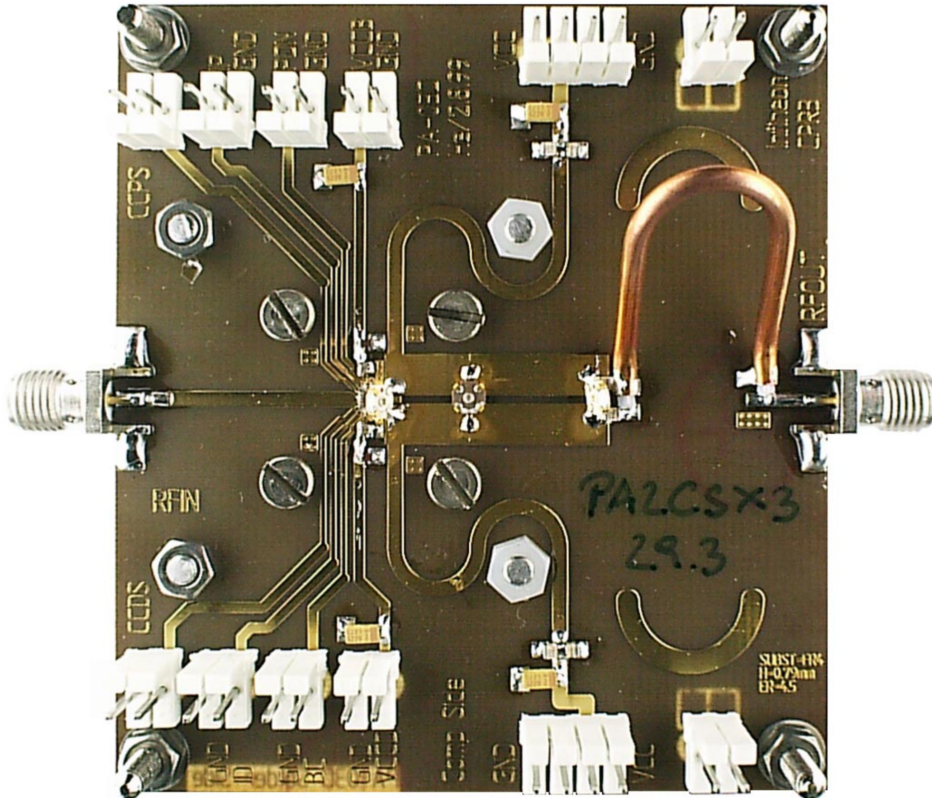

Figure 26: Photograph of the power amplifier FR4 test board including heat-slug (board size: 70 mm x 78 mm).

gain is 38 dB. The maximum output power at 4.5 V supply voltage is 7.5 W at a PAE of

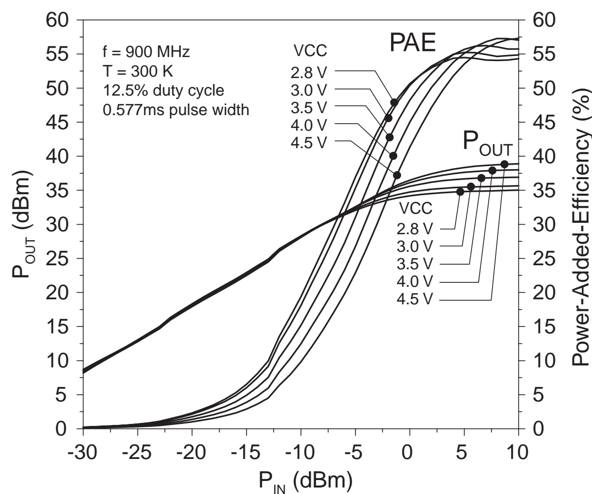

Figure 27: Measured output power and PAE versus input power and supply voltage.

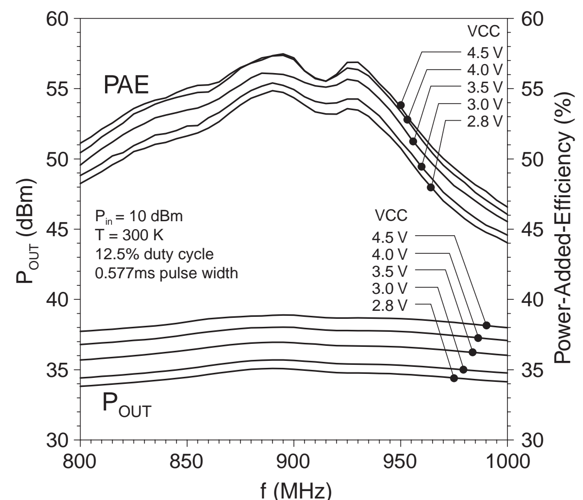

Figure 28: Measured output power and PAE versus frequency.

57 %. The collector efficiency of the output stage is 68 % in this case. But at this high level of output power, load impedance mismatch can result in damage of the output stage. However, at an output VSWR=10 the maximum usable supply voltage is 3.5 V. Output

Operating frequency	800 - 1000	MHz
Supply voltage	2.8 – 4.5	V
Maximum output power (at 2.8 V / 4.5 V and 900 MHz)	3.2 / 7.7	W
Maximum PAE (at 3.2 W / 7.7 W and 900 MHz)	54 / 57	%
Output-stage collector efficiency (at 3.2 W / 7.7 W and 900 MHz)	66 / 68	%
Input VSWR (at 900 MHz, single-ended input signal)	1.7	
Small-signal gain	38	dB

Table 2: Characteristics of the 900 MHz monolithic Si bipolar power amplifier.

power and PAE versus frequency are shown in Fig. 28. The 3rd-order output intercept point is +41.3 dBm at 900 MHz and 3 V supply voltage. Table 2 gives a summary of the power amplifier performance.

5. A LUMPED LC-BALUN AS OUTPUT MATCHING NETWORK

Fig. 29 shows a lumped LC balun, which was originally used as an antenna balun [6, 16, 17]. This circuit can be used as a simple output matching network for push-pull type power amplifiers. However, the PAE-performance of the power amplifier is limited due to inappropriate impedances at the harmonic frequencies. The performance of a lumped LC balun at 900 MHz and 4 W output power is evaluated in [7].

The bridge-type circuit (Fig. 29) consists of two inductors $L_1 = L_2$ and two capacitors $C_1 = C_2$. A rf-choke coil and a dc-block capacitor is used to feed the supply voltage.

R_1 is the balanced input impedance of the bridge. Each collector is loaded by $R_1/2$. R_L is the load resistor, 50 Ω usually. L and C can be calculated by

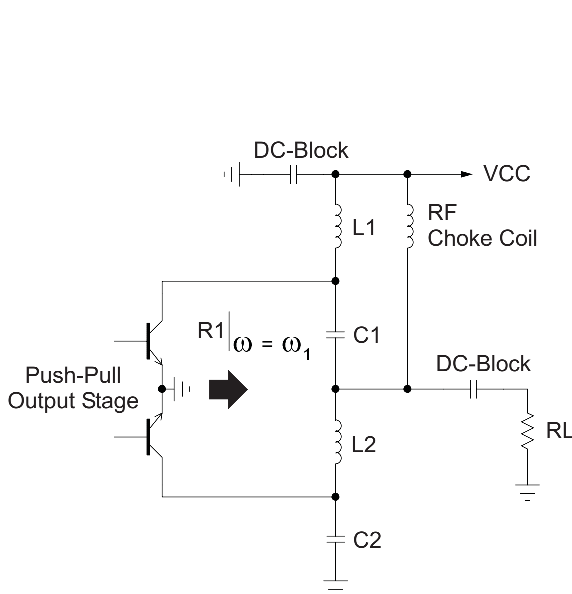

Figure 29: Lumped LC balun network.

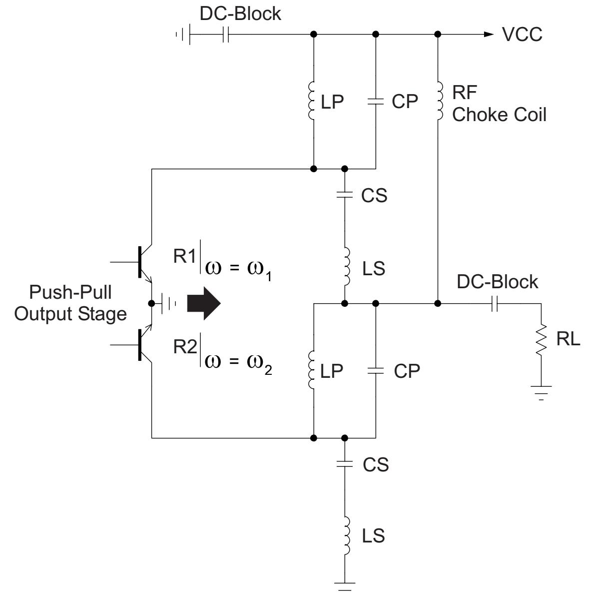

Figure 30: Dual-band lumped LC balun.

$$L_1 = L_2 = \frac{Z_1}{\omega_1} \tag{19}$$

$$C_1 = C_2 = \frac{1}{\omega_1 Z_1} \tag{20}$$

where $Z_1 = \sqrt{R_1 \cdot R_L}$ is the characteristic impedance of the bridge-type circuit. $\omega_1 = 2\pi f_1$ is the frequency of operation. R_1 and Z_1 are assumed to be real valued. If R_1 should be complex valued, matching is possible, but then the bridge becomes more or less imbalanced ($C_1 \neq C_2$ and $L_1 \neq L_2$). Better performance and less sensitivity against changes in component values can be achieved, if the imaginary part of the optimum load impedance is matched separately using a simple additional transformation network (L, C or LC) connected in series or in parallel to the output of the power amplifier.

If the inductors are replaced by a parallel resonant circuit and the capacitors are replaced by a series resonant circuit in Fig. 29, then a lumped dual-band LC balun, shown in Fig. 30, is available.

The circuit provides a balanced input impedance R_1 at $\omega_1 = 2\pi f_1$ and R_2 at $\omega_2 = 2\pi f_2$. Independent matching and balun conversion at two different frequencies can be done. L_S, C_S, L_P and C_P can be calculated by

$$L_S = \frac{\omega_1 \cdot Z_1 + \omega_2 \cdot Z_2}{\omega_2^2 - \omega_1^2} \tag{21}$$

$$C_S = \frac{\frac{\omega_2}{\omega_1} - \frac{\omega_1}{\omega_2}}{\omega_1 \cdot Z_2 + \omega_2 \cdot Z_1} \tag{22}$$

$$L_P = \frac{\left(\frac{\omega_2}{\omega_1} - \frac{\omega_1}{\omega_2}\right) \cdot Z_1 \cdot Z_2}{\omega_1 \cdot Z_1 + \omega_2 \cdot Z_2} \tag{23}$$

$$C_P = \frac{\omega_1 \cdot Z_2 + \omega_2 \cdot Z_1}{(\omega_2^2 - \omega_1^2) \cdot Z_1 \cdot Z_2} \tag{24}$$

where $Z_1 = \sqrt{R_1 \cdot R_L}$ and $Z_2 = \sqrt{R_2 \cdot R_L}$ are the characteristic impedances of the bridge at ω_1 and ω_2. R_1, R_2, Z_1 and Z_2 are assumed to be real valued. Note, that

$$\omega_2 > \omega_1 \tag{25}$$

is a must, using the design equations above.

6. CONCLUSION

A study is presented of the electrical characteristics of lumped planar transformers. A precise lumped low-order equivalent model is derived from the physical layout. Measurement and model shows excellent agreement.

For the first time, transformer-coupled push-pull type power amplifiers with a high performance are integrated in Si-bipolar at 900 MHz and 2 GHz.

REFERENCES

[1] G. Rabjohn, *Balanced Planar Transformers.* United States Patent with Patentnumber 4,816,784, 1989.

[2] J. Long, "Monolithic Transformers for Silicon RF IC Design," *IEEE of Solid-State Circuits*, vol. 35, pp. 1368–1382, September 2000.

[3] J. McRory *et al.*, "Transformer Coupled Stacked FET Power Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 157–161, February 1999.

[4] J. Long *et al.*, "A 5.1-5.8 GHz Low-Power Image-Reject Downconverter in SiGe Technology," in *Proceedings of the 1999 Bipolar/BiCMOS Circuits and Technology Meeting*, (Minneapolis), pp. 67–70, September 1999.

[5] H. Wohlmuth *et al.*, "2 GHz Meissner VCO in Si Bipolar Technology," in *29th European Microwave Conf., Conf. Proc., Vol. 1*, (Munich), pp. 190–193, October 1999.

[6] S. Cripps, *RF Power Amplifiers for Wireless Communications.* Norwood, MA 02062: Artech House, first ed., 1999.

[7] Simbürger, W. *et al.*, "A Monolithic Transformer Coupled 5 W Silicon Power Amplifier with 59 % PAE at 0.9 GHz," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 1881–92, December 1999.

[8] W. Simbürger *et al.*, "A Monolithic 2.5V, 1W Silicon Bipolar Power Amplifier with 55% PAE at 1.9GHz," in *IEEE MTT-S International Microwave Symposium Digest*, (Boston), pp. 853–856, IEEE, June 2000.

[9] A. Heinz *et al.*, "A Monolithic 2.8V, 3.2W Silicon Bipolar Power Amplifier with 54% PAE at 900MHz," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium Digest of Papers*, (Boston), pp. 117–120, IEEE, June 2000.

[10] MIT, *FastHenry USER's GUIDE, Version 3.0.* Massachusetts Institute of Technology, 1996.

[11] MIT, *FastCap USER's GUIDE.* Massachusetts Institute of Technology, 1992.

[12] D. Kehrer, "Design of Monolithic Integrated Lumped Transformers in Silicon-based Technologies up to 20 GHz," Master's thesis, Technical University of Vienna, Institute of Communications and Radio-Frequency Engineering, Gusshausstrasse 25/389, A-1040 Vienna, Austria, December 2000.

[13] Böck, J. *et al.*, "A 50 GHz Implanted Base Silicon Bipolar Technology with 35 GHz Static Frequency Divider," in *Symposium on VLSI Technology, Digest of Technical Papers*, pp. 108–109, 1996.

[14] Rickelt, M. and Rein, H.-M., "Impact-Ionization Induced Instabilities in High-Speed Bipolar Transistors and their Influence on the Maximum Usable Output Voltage," in *Bipolar/BiCMOS Circuits and Technology Meeting*, (Minneapolis), pp. 54–57, IEEE, September 26-28 1999.

[15] Klose, H. *et al.*, "B6HF: A 0.8 Micron 25 GHz / 25 ps Bipolar Technology for "Mobile Radio" and "Ultra Fast Data Link" IC Products," in *IEEE Bipolar Circuits and Technology Meeting*, pp. 125–127, IEEE, 1993.

[16] A. Krischke, *Rothammels Antennenbuch.* Stuttgart: Franck-Kosmos, 11th ed., 1995.

[17] P. Vizmuller, *RF Design Guide - Systems, Circuits, and Equations.* Norwood, MA 02062: Artech House, first ed., 1995.